SEMINAR
TECHNISCHER BEREICH

Datum: Dienstag, den 23.04.2002, 10.00 Uhr

Ort: DESY Zeuthen, Seminarraum 2

Thema: **Front-end Electronics for the CMS Muon Strip Chambers**

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Front–end Electronics for the CMS Muon Strip Chambers

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ME1/1 Requirements

Front - End electronics optimized for required performance and experimental condition of ME1/1 CSC's:

Spatial resolution	75μm
Timing resolution	2÷3ns
Non uniform magnetic field	~3Tesla
Background rates	~100kHz/channel

ME1/1 Front - End ASIC's for cathode and anode readout boards:

	Function	Number of readout channels (chips)	Total number of chips to be produced
Cathode	accurate measurements of induced strip charge in order to provide high spatial resolution	48384 (3024)	4500
Anode	high timing resolution for bunch crossing's identification	20736 (2592)	3500

ME1/1 Readout Electronics General Features

ME1/1 Front – End

	CATHODE ASICs	**ANODE ASICs**
MAIN FUNCTIONS:	• to provide accurate measurements of induced strip charge (DAQ) • to provide high timing resolution for cathode trigger signal (Trigger)	• to provide high timing resolution for BX identification

Requirements to ME1/1 Front-end performance

Rate capability	>100kHz/strip
Response to 1MIP/Noise ratio (for DAQ channel)	>100
Dead time after 500MIP overload	<5μs
Comparator threshold (to provide time resolution)	5-10fC
Power consumption	<25mW/chan
Total number of readout channels:	
Cathode front-end electronics	**~56000**
Anode front-end electronics	**~24000**

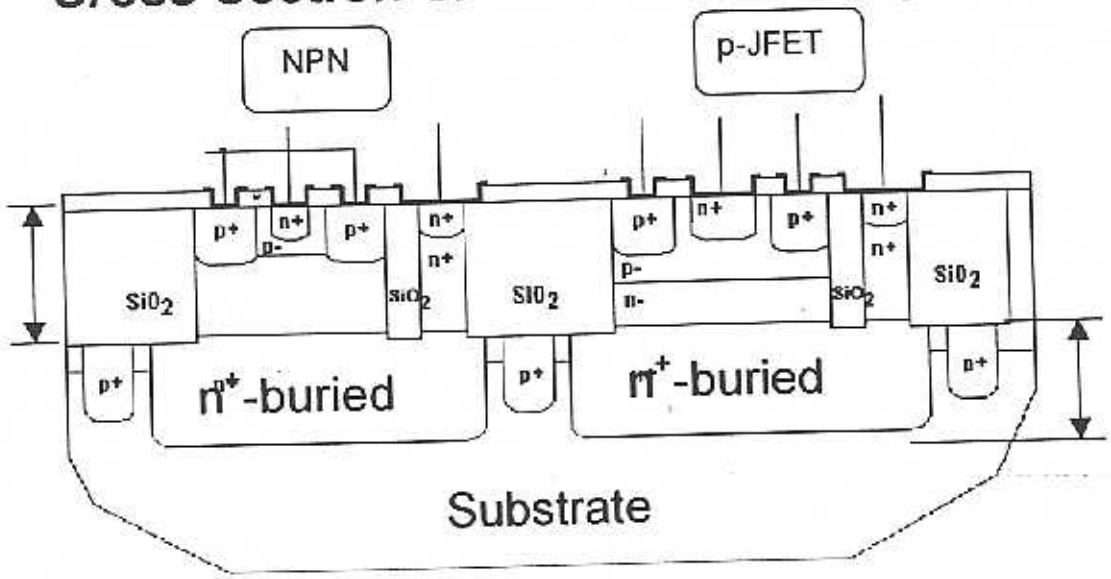
Microwave Bi-jFET Technology

Specific design and technology solutions are used to decrease sènsitivity to radiation damage:

- Most radiation – hard transistors with ***vertical*** structure are used in design: microwave ***npn***s and ***p-jFET***s.
- High injection level.
- Epitaxial lays.
- SiO_2 trench isolation.
- Guardrings between adjacent channels and some critical functional blocks.
- Lots of **substrate** and **well** contacts.

Microwave Bi-jFET Technology

Cross-section of main active components



Main Features

- 1.2μ design rules.
- Active components: *npn* , *p-jFET*.
- Passive components: MOS capacitors, active base p^- - resistors.
- SiO_2 trench isolation.

ME1/1 Cathode ASIC prototyping

"KATOD-1" and "KATOD-2" development goals:

- Choice of head device and optimization of preamplifier.
- Optimization of the *tail cancellation* and shaper gain.
- Shaper peaking time optimization.

Main result of the beam testing (CERN, P3-P4 prototype):
ME1/1 instrumented with Minsk ASICs can operate at low gas gain in the range of $(5 \div 7) \times 10^4$ with spatial resolution ~100 μm
(in presence of input background rate ~100kHz/strip)

"KATOD-1m" development goal:

Testing of the ***base line restoration*** technology.

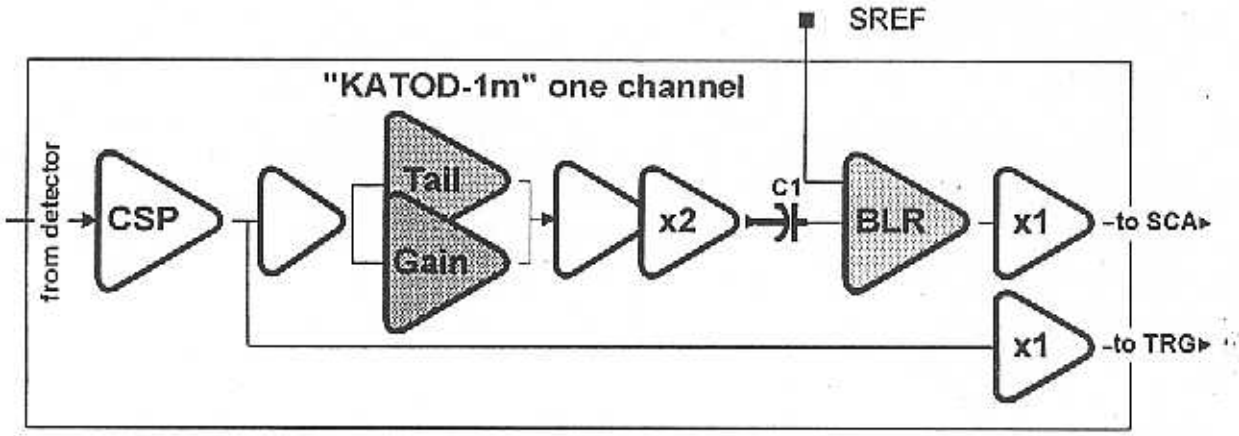
Main result of rate capability test (X-ray test setup, Dubna):
ASIC can operate at 1MHz input rate with recovery time of output pulse ~500ns.

"KATOD-5" (final submission) development goal:

Compatibility with the "Buckeye" chip:

- The same Power supply and reference levels.
- The same package type.
- "Pin - to – pin" compatibility
- Optimisation to the new chamber geometry.

For cathode readout one of the main task is to provide proper tail cancellation in order to obtain optimal signal-to-noise ratio in presence of high input rates. The gain of ME1/1 cathode amplifier is supposed to be in the range of 4 – 8 mV/fC. The result of R&D is "KATOD-1m" ASIC, which block diagram is shown at fig.



Main Electrical Characteristics

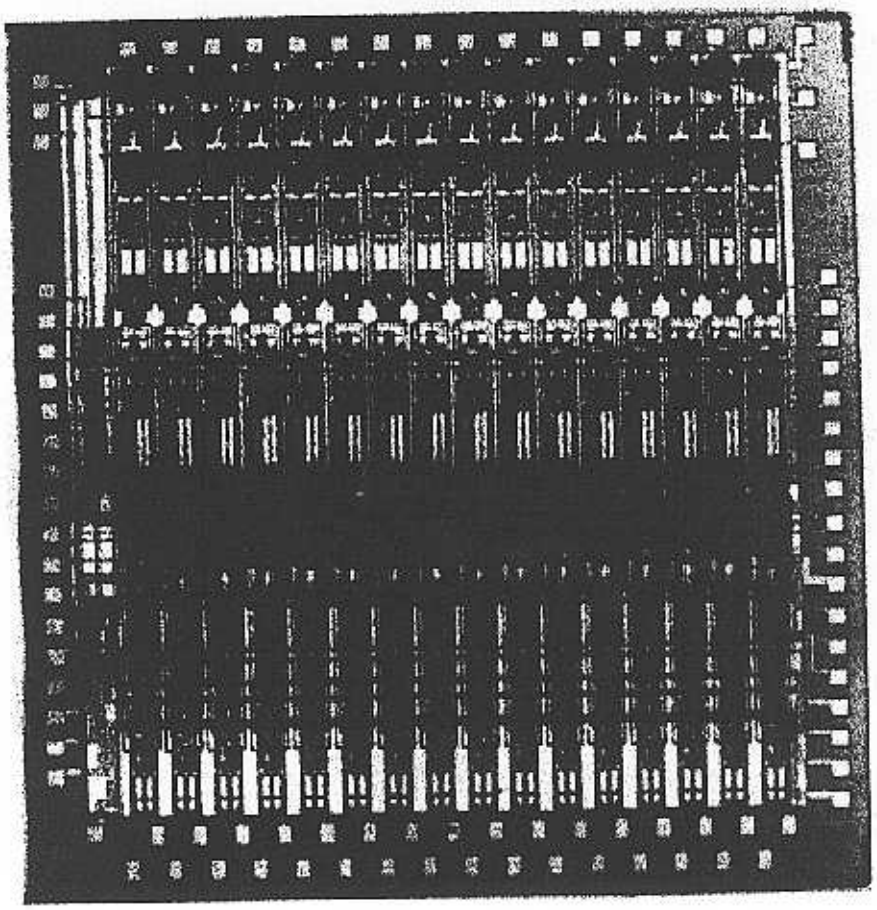
Charge sensitive preamplifier

Feedback Resistor	100	kOhm
Feedback Capacitor	1.5	pF
Transient Response Rise Time Cd=100pF	12	ns

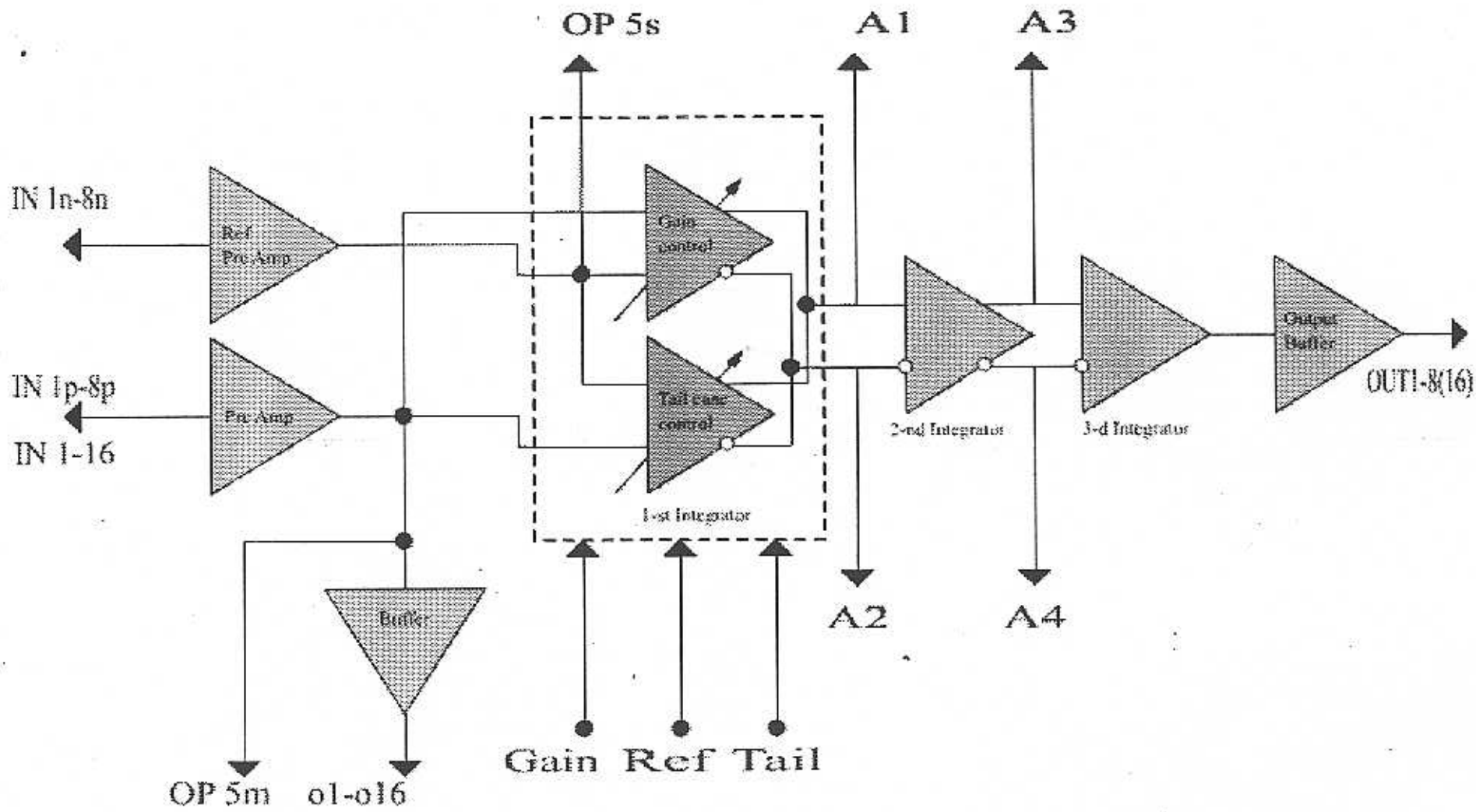
Amplifier - shaper

Gain control range	0.5 ... +10	mV/fKl
Gain control voltage range	0 ...+1	V
Tail Cancelation control voltage range	0 ...+1	V
Output pulse peaking time Cd=100pF	110	ns
Power consumption	<30	mW/channel
ENC (r.m.s.) Cd=0	3000	e
ENC slope	+10	e/pF

KATOD-1 ASIC Layout



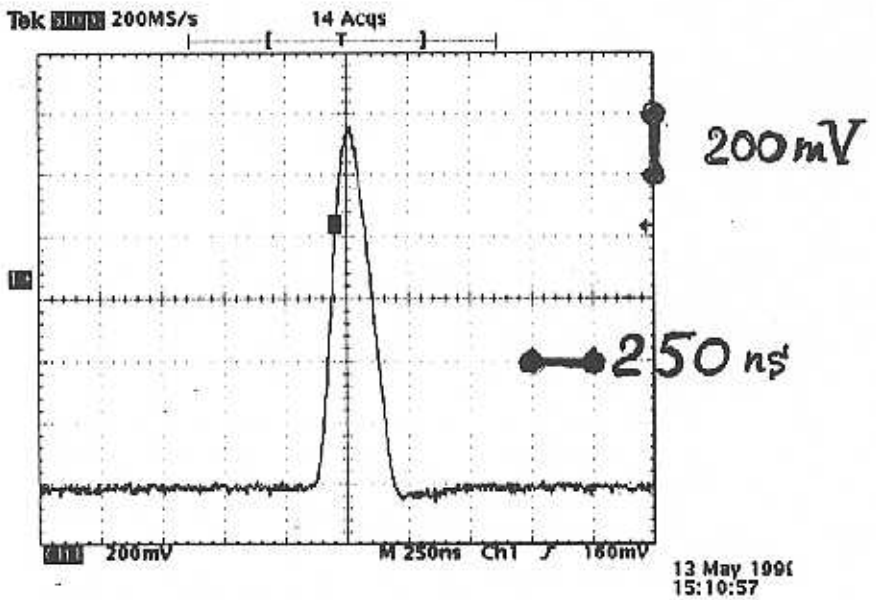
- *Technology 1.2 μm, Bi-jFET*
- *Die dimensions 5.2 x 4.6 mm.*



"KATOD1" BLOCK DIAGRAM

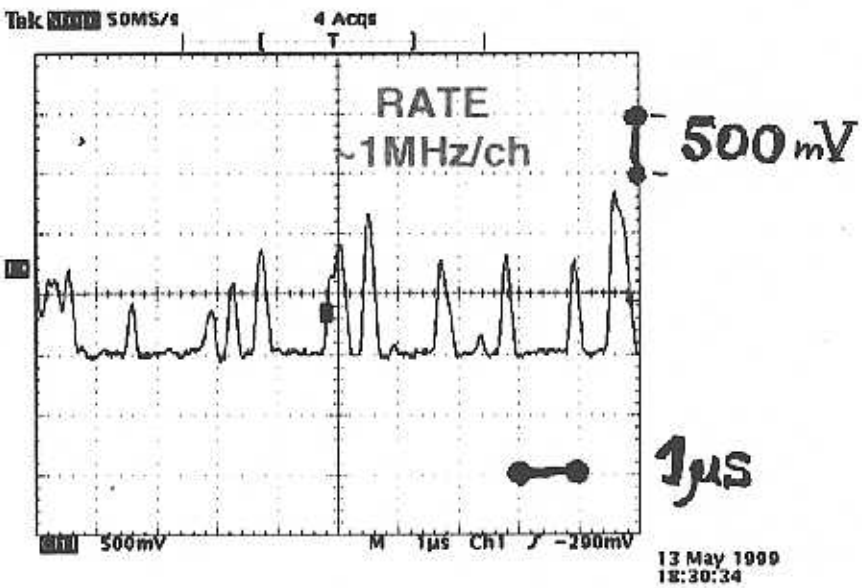
ME1/1 Cathode Front–End ASIC R&D

Rate capability test of KATOD-1m ASIC
Dubna, May 1999, X-ray test setup.



ASIC Output Signal.

Peaking Time ~150ns
Recovery Time ~500ns



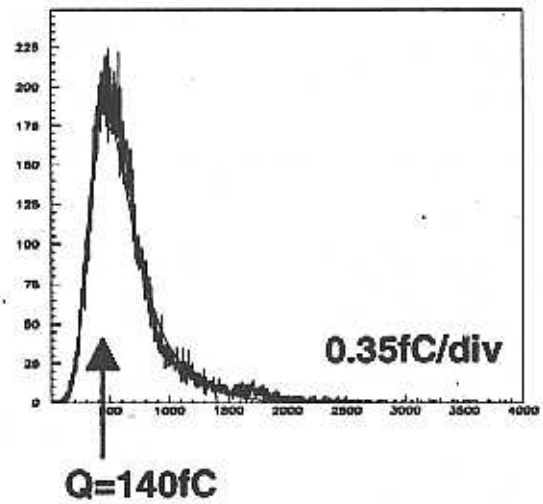
ASIC Output Signal.

Shift of output base line not exceeds 40mV.

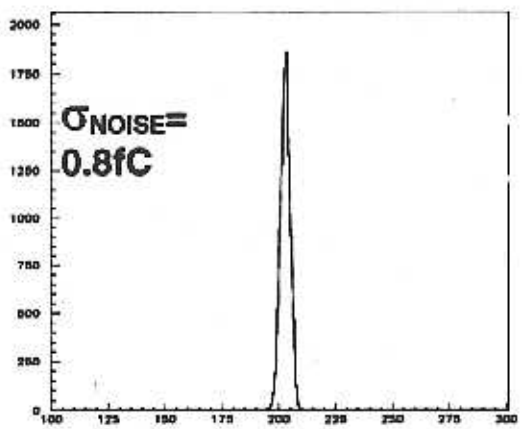
ME1/1 cathode front-end chip experimental results

(P3 Prototype Beam Test, H2, CERN, 1997)

Typical cathode charge distribution ("KATOD-1" ASIC)

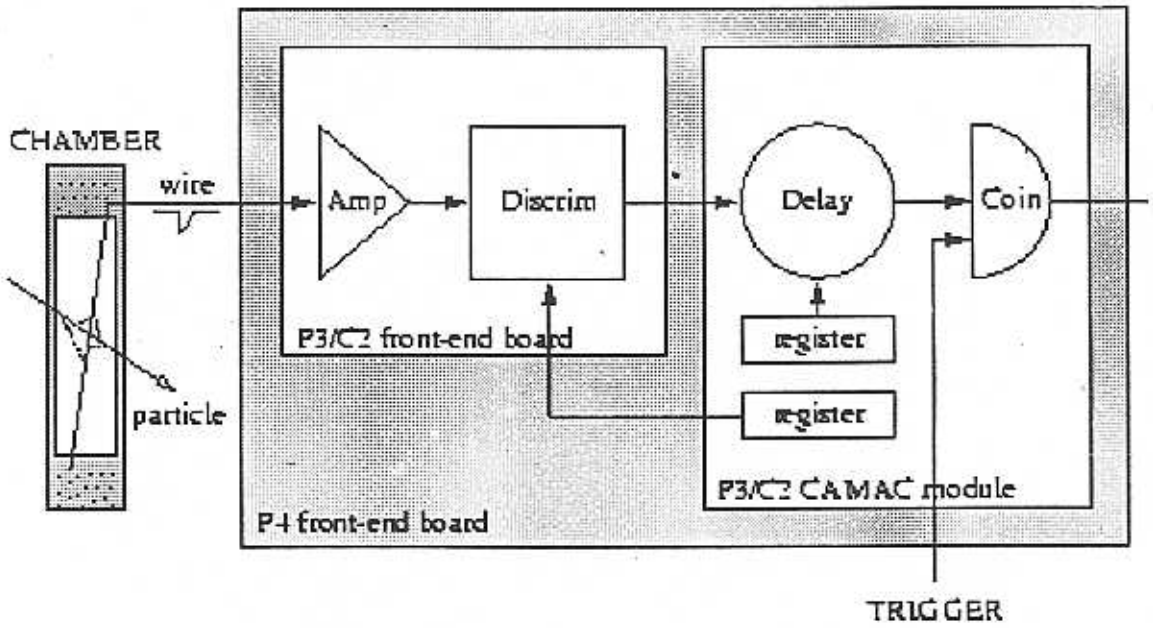


Pedestal distribution



"Signal to noise" ratio ~175

(Ua~2.95kV, Gas Gain~10^5)



PCOS4-like onchamber electronics being implemented now by NC PHEP for Oka experiment (Protvino, Russian Federation). Front-end chip is originally developed, produced and successfully tested on the beam by electronics experts of NC PHEP. Digital part is being implemented with Altera chip MAX7000.

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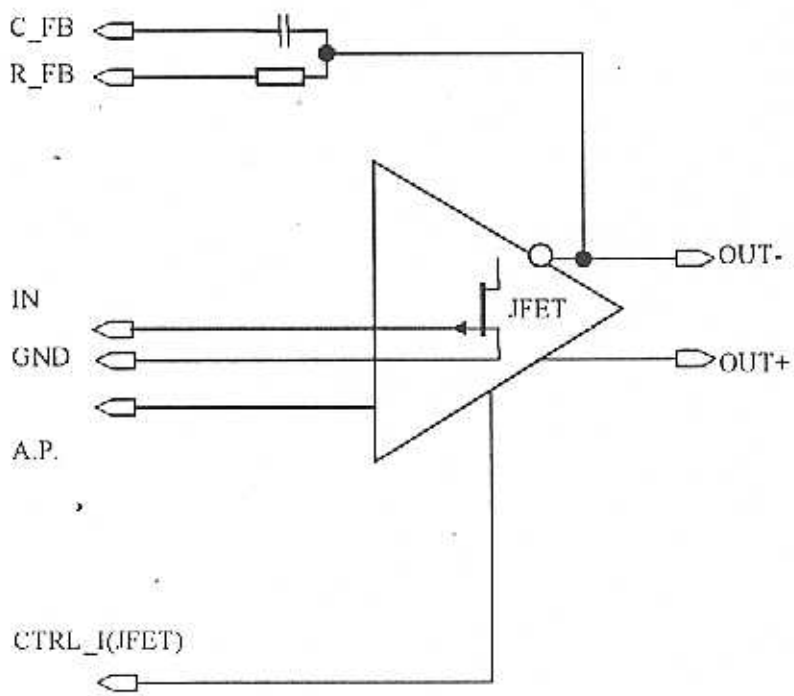
Low-noise Wideband Pulse Preamplifiers for Low Capacitance Signal Source.

Equivalent noise charge less then 1000 electrons at the width of pulse 80 ns
Output signal by amplitude up to 2V on load 50 Om
Nano- and microseconds of shaping times



The chip is packaged as a 14-pin PLCC for high density surface mount printed circuit boards.

IC provides:

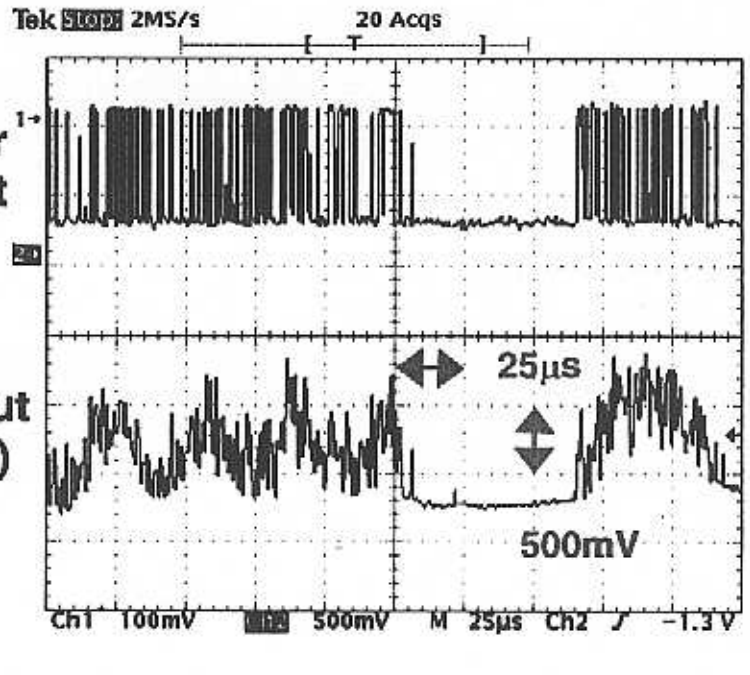
- *readout of analog data with detector of ionizing radiations;*
- *conversion of input signal current into output voltage;*
- *amplification as to voltage of wideband impulse signal.*

Table 2

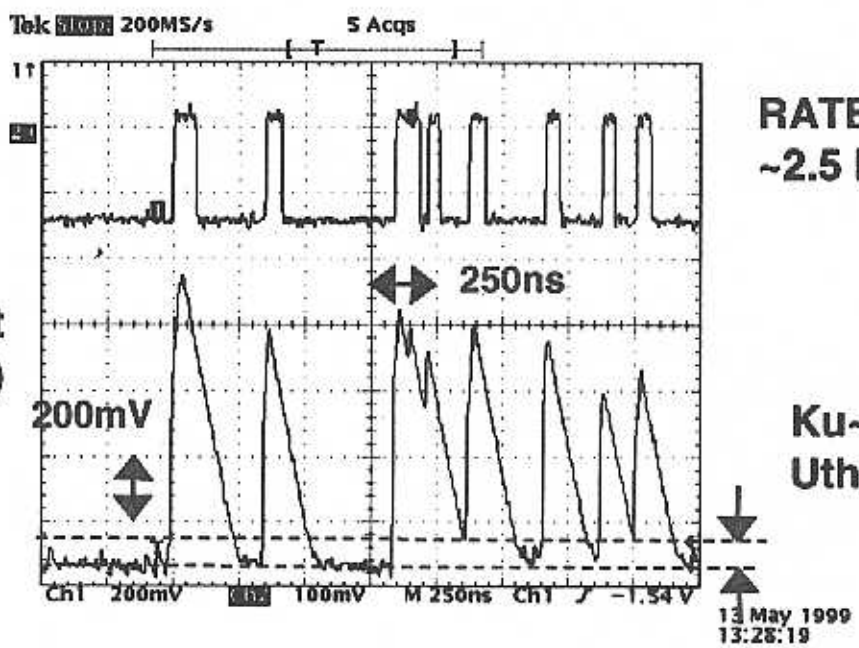
Name	Pinout Number(s)	Description
In1÷In8	35,37,39, 41, 43,45,47, 2	Signal inputs
In_t	32	Test input, Ctest=0.2pF
Op1÷Op8; On1÷On8	11÷26	Positive and negative LVDS compatible outputs
Out_p_8ch	8	Positive shaper output of 8 channel (before BLR)
Th_ctrl	29	Threshold control, control voltage range from 0 up 0.5V
Mps	6	Mirror bases of shapers
Mbdo	7	Mirror bases of BLRs and discriminators
Mamp	10	Mirror bases of LVDS drivers
In_ref	34	Input of reference preamplifier
Vref	31	Output of reference preamplifier (reference level for shapers)
Vcc	28	Preamplifiers and shapers positive supply (+5V)
Vcc1	27	BLRs and discriminators positive supply (+5V)
Vee	5	Ground shapers (substrate)
Gnd	4,33	Ground of preamplifiers
Vee1	9	Ground of BLRs and discriminators
	36,38,40, 42, 44,46,48, 1, 3	Free pinouts (Connect better to ground.)

ME1/1 anode front-end chip rate capability test (X-ray test, Dubna, 1999)

"ANOD-1m" ASIC output signals



RATE
~10 MHz/ch

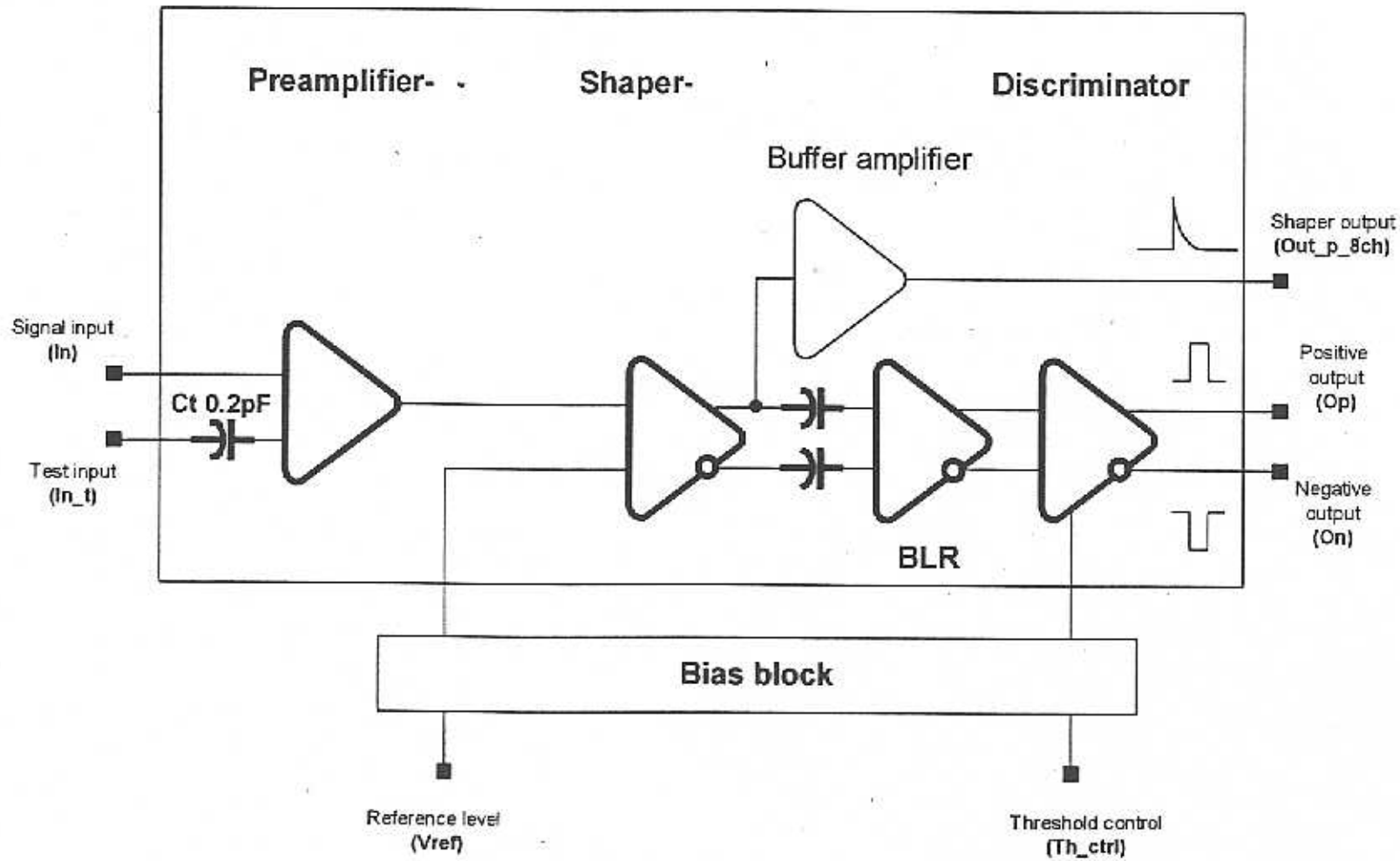


RATE
~2.5 MHz/ch

Ku~10mV/fC
Uth~8fC

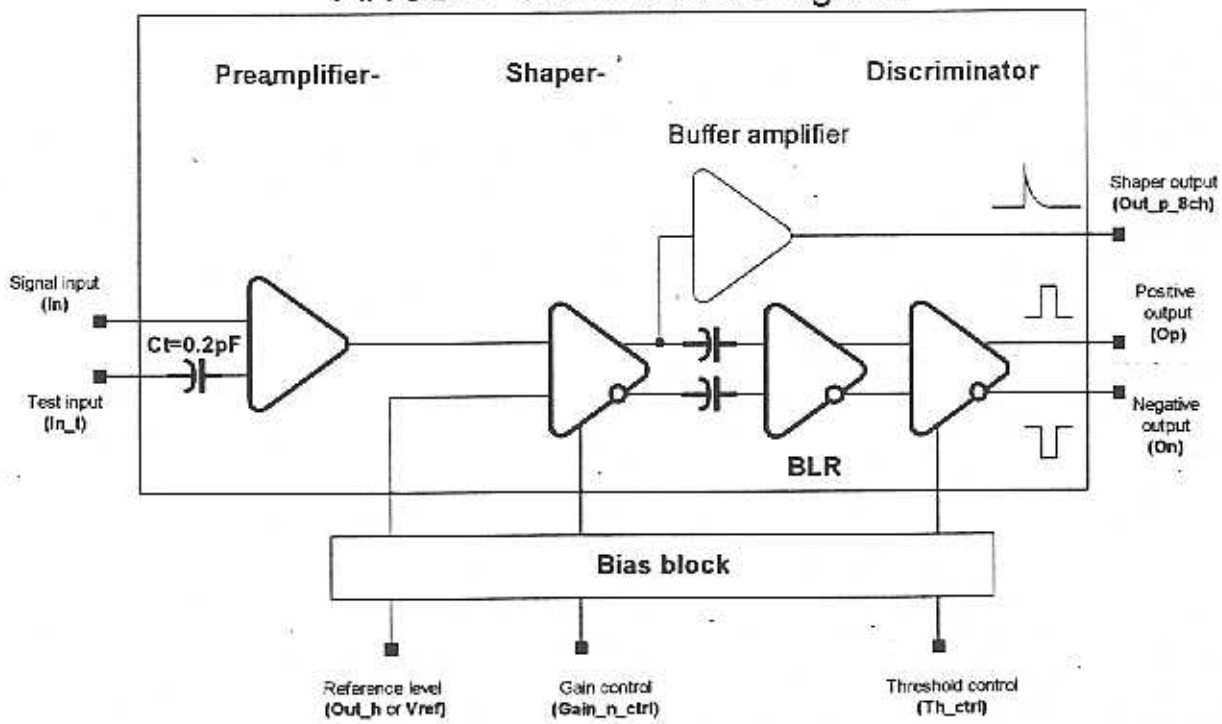
Double Pulse Resolution ~100ns

"Anode-2m" ASIC Channel Block Diagram
(June 2001)



ASICs for CSC anode readout

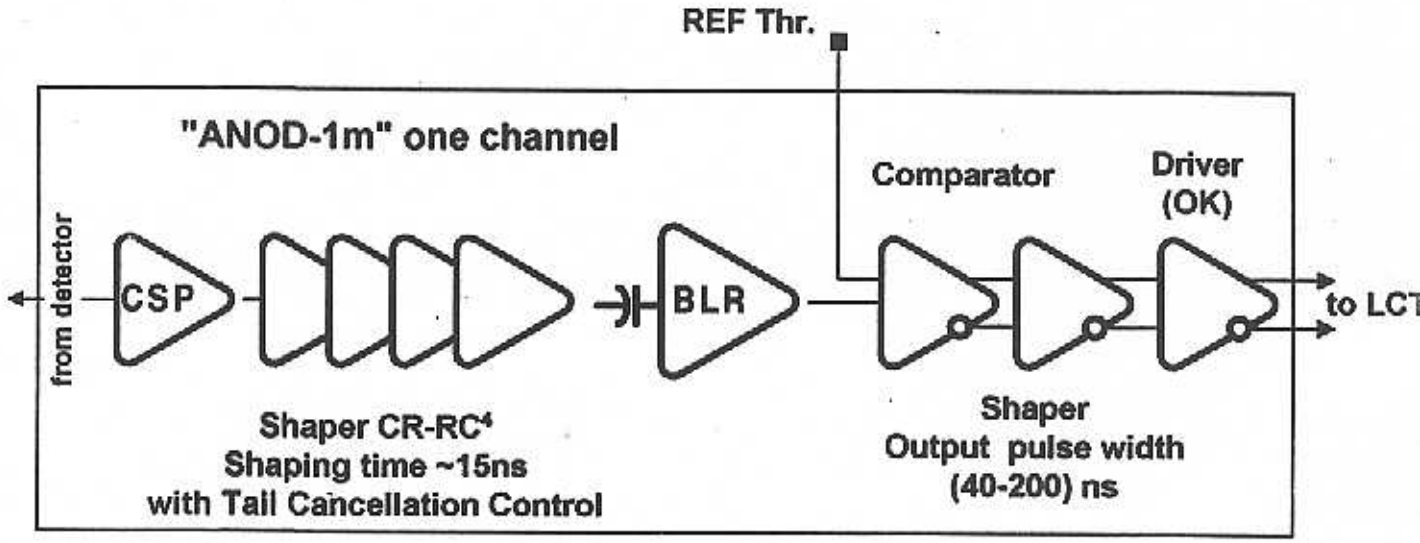
"ANOD-2" ASIC block diagram



"Anod-2" main specifications

Noise, ENC (r.m.s.) @100pF	4500 e
Gain	10mV/fC
Rate capability	10 MHz
Recovery time @ 250pC overload	2 μs
Threshold range	(5÷50) fC
Output levels	LVDS

ME1/1 Anode Front- End Chip Block Diagram



- 8- channels ASICs
- Shaper CR-RC^4 with Tail Cancellation
- Minimal comparator threshold ~8fC
- ENC (r.m.s) ~1600+20e/pF

ME1/1 Anode ASIC Prototyping

"ANOD-1" development goals:

Amplifier optimization for the ME1/1 CSC:

- shaper peaking time;
- gain;
- tail cancellation.

Main results of the beam testing (CERN):

- time resolution σ = 2.7ns;
- anode layer efficiency ~100%.

"ANOD-1m" development goals:

Inserting of the base line restorer to the channel in order to increase rate capability and to decrease threshold spread range.

Main results of the X – ray testing (Dubna):

- double pulse resolution ~100ns.

Conclusion:

The anode ASIC R&D results show that the chip meets to the ME1/1 requirements.

ASICs for CSC anode readout

Chip for Anode very front – end readout

1995 – 1999 R&D several prototypes of 8 channels charge sensitive preamplifier-shaper-discrimitator IC:

"ANOD-1":

- Optimization of preamplifier
- Choice of tail cancellation method
- Optimization of shaper peaking time and gain
- Beam testing (with ME1/1 P3 prototype)

"ANOD-1m":

- Inserting of the base line restorer in order to decrease threshold distribution and improve input rate capability
- Rate capability testing (with ME1/1 P0 prototype)

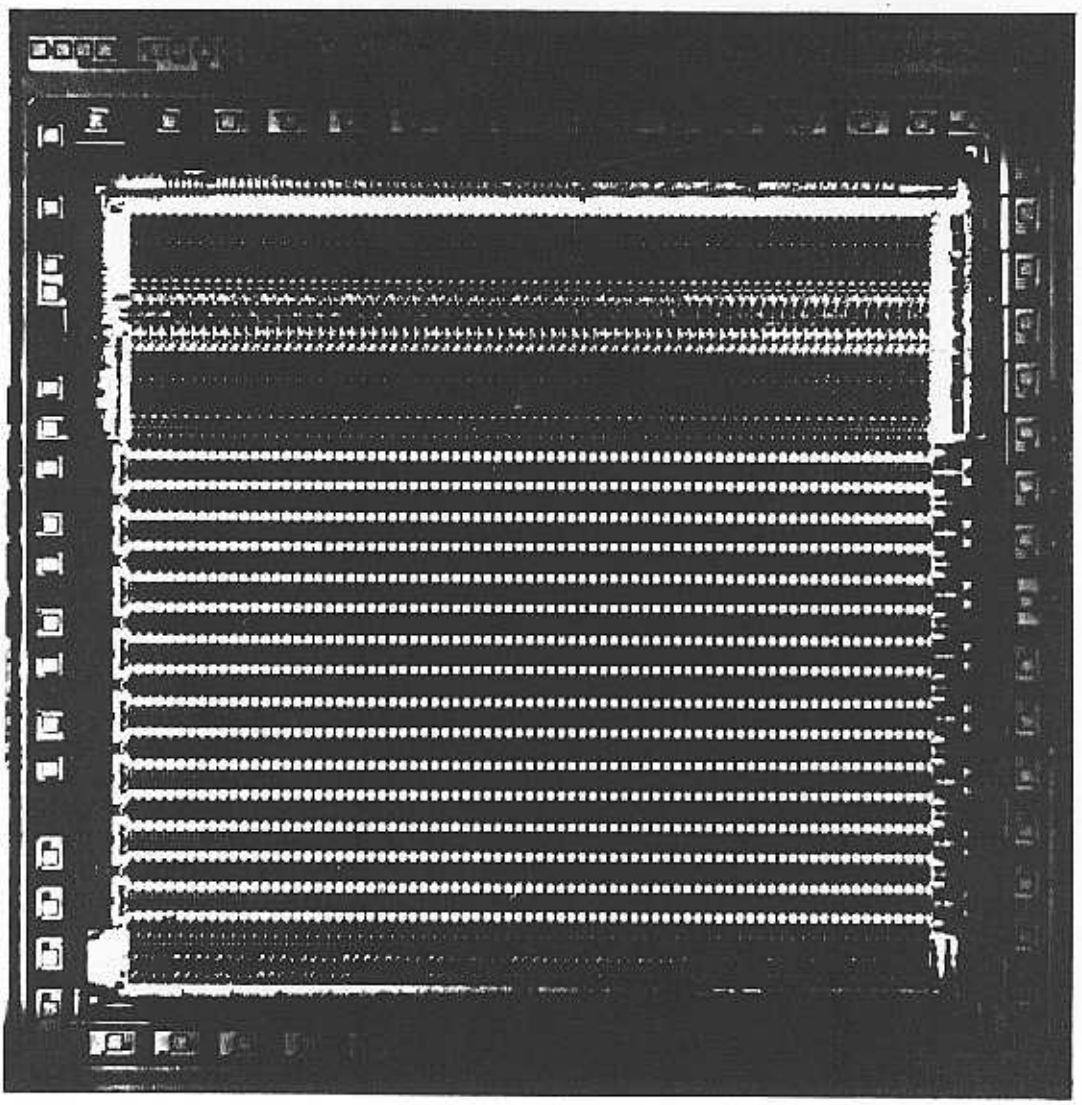
"ANOD-2" (final submission):

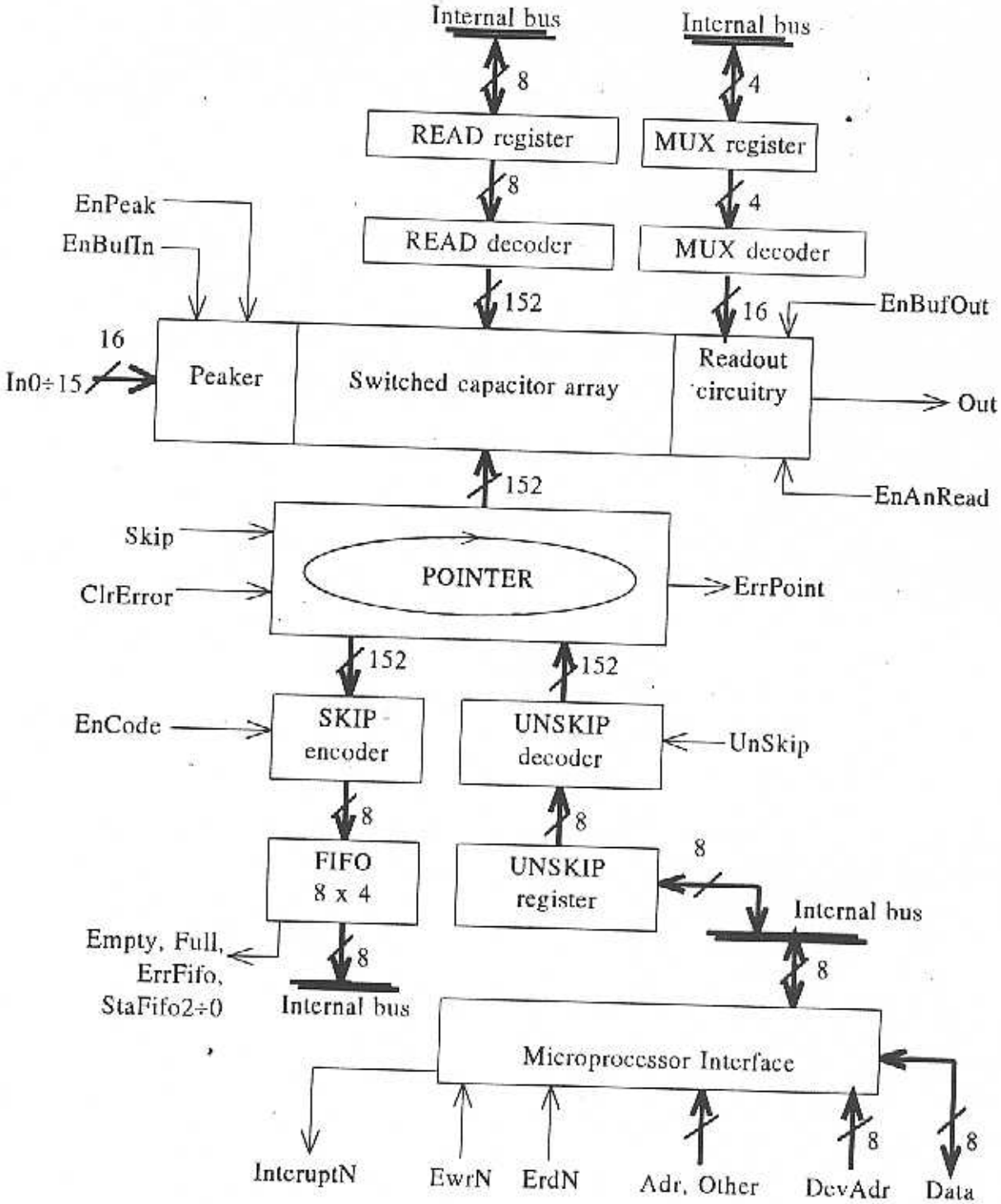
- LVDS output levels
- Single +5 volt operation

"AnMem-1" chip

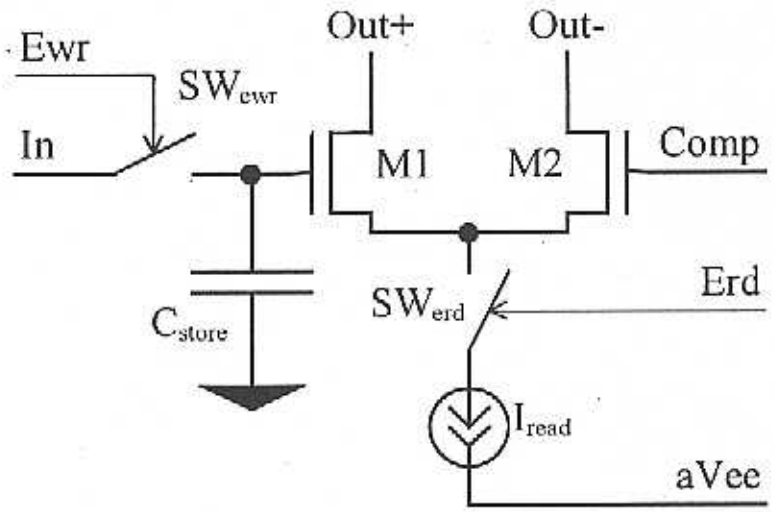
16×152 cells

1.5 µm *CMOS*

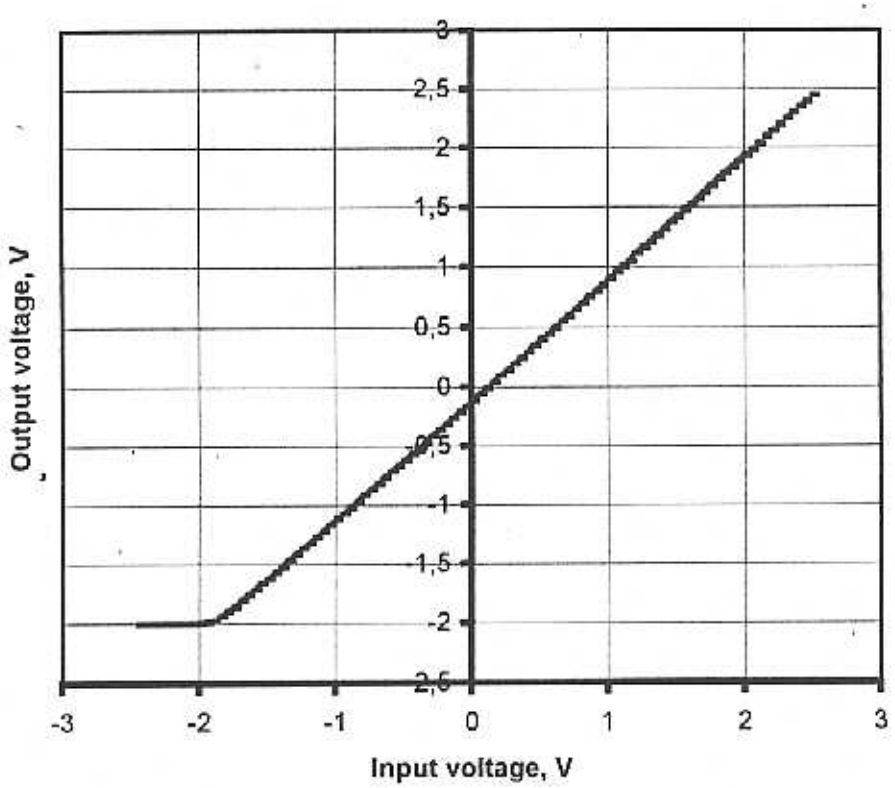




Block diagram of memory unit



Simplified schematic of one memory cell.



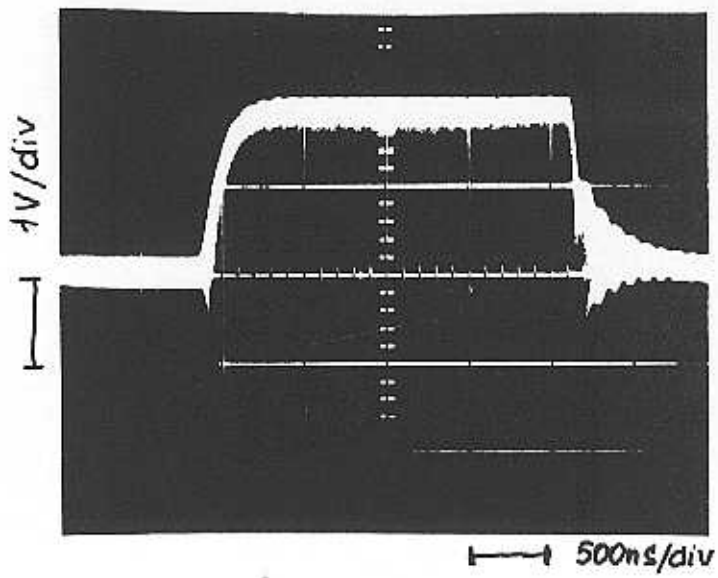
AnMem1's cell dynamic range. Integral nonlinearity is better then 1%.

Analog Memory IC

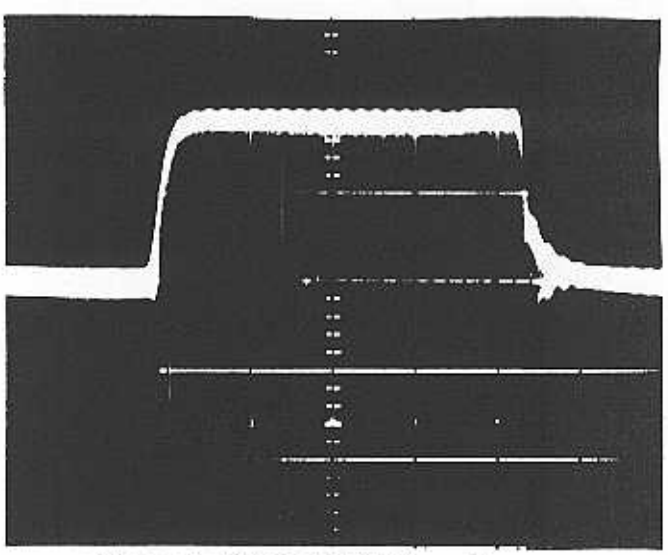
'Cathode-1' (*First Iteration, 16×152-cells*)

Results of testing.

A)



B)



Track / Hold / Track

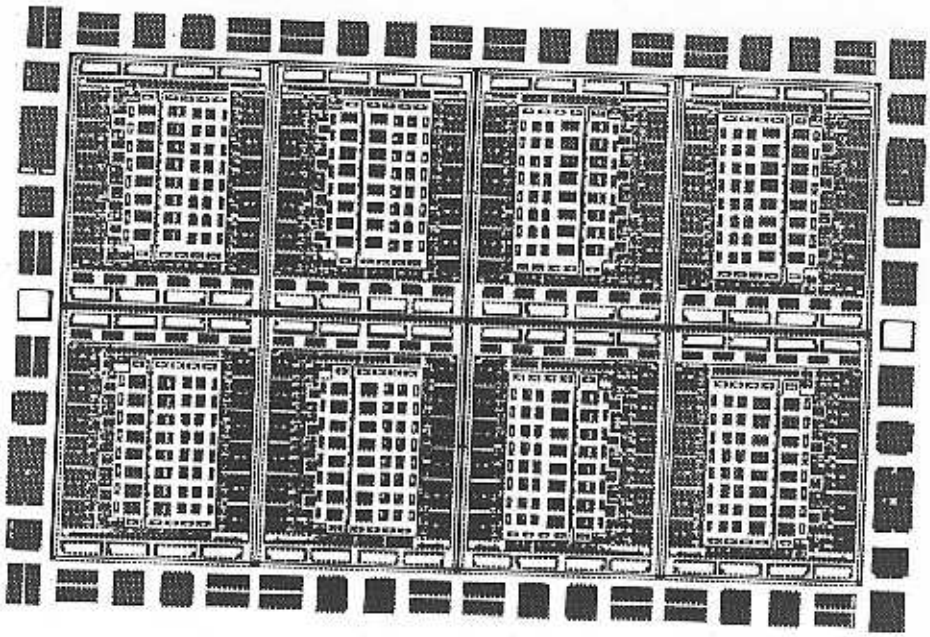
Input signal: sinusoidal voltage, amplitude= 2V, frequency=10 MHz.

A) output buffer disabled,

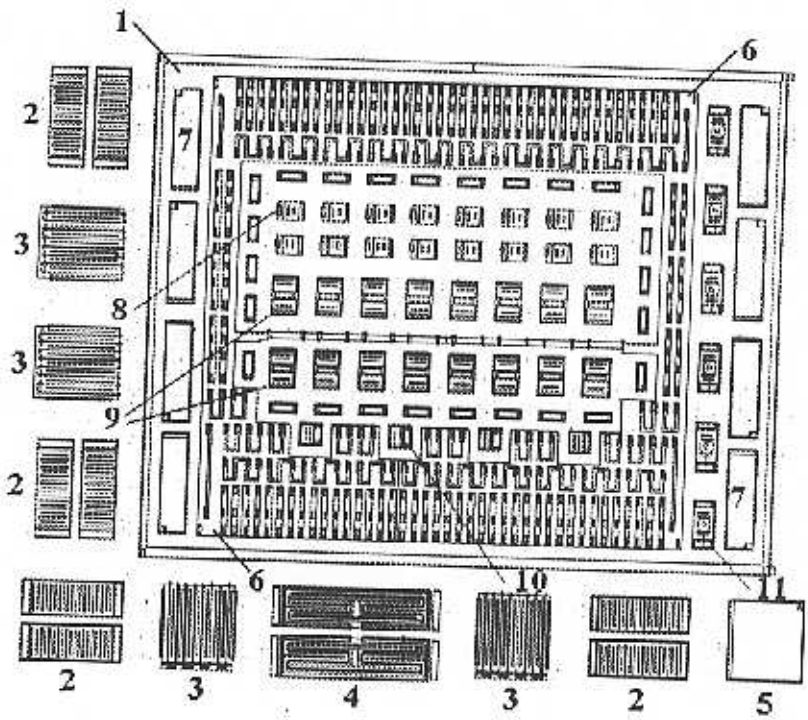
B) output buffer enabled,

storage cell discharge time constant ≥70 seconds

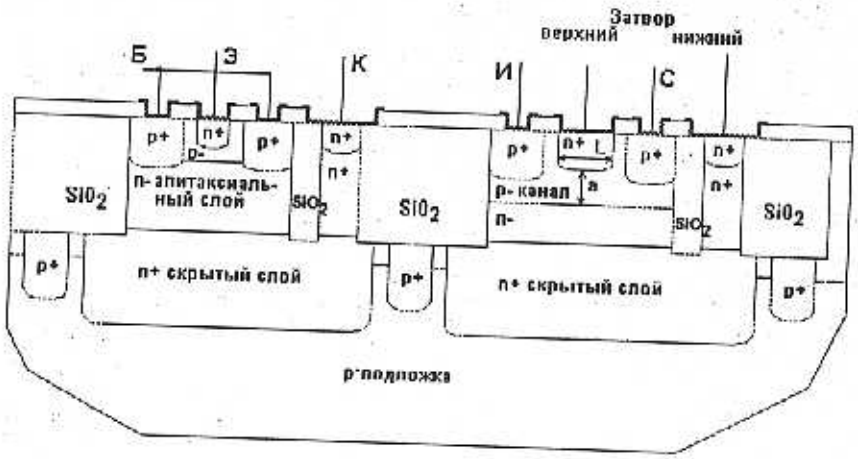
Mask programmable analog array



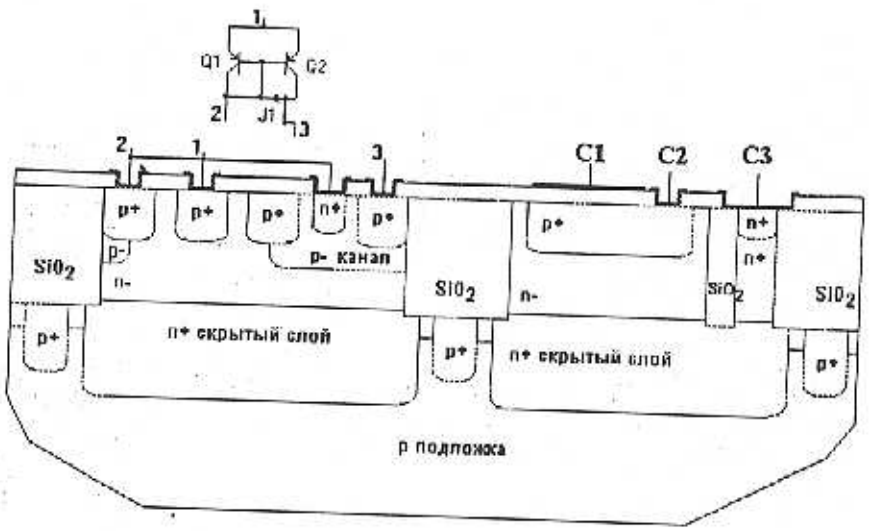
Single tile

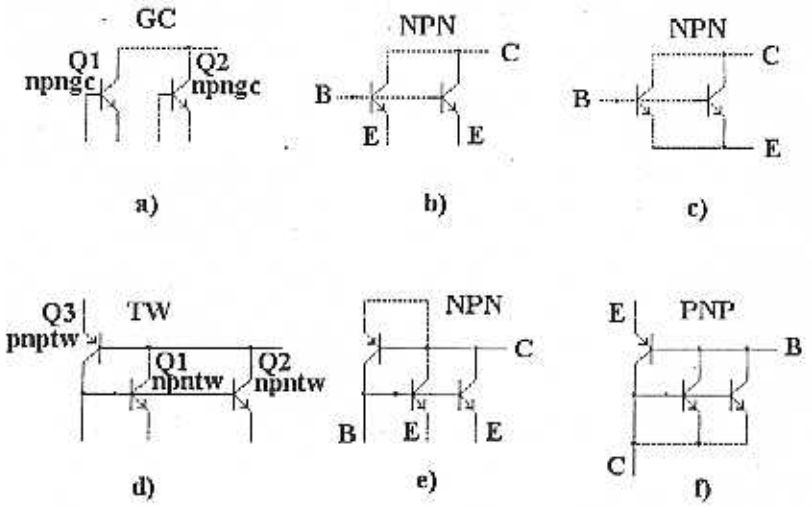


Vertical section of single *npn* and *jFET*

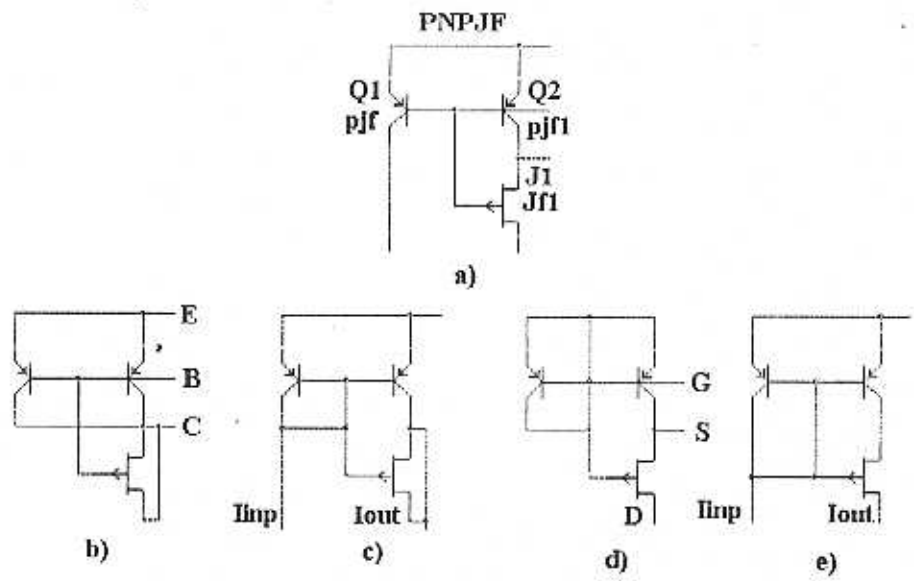


Vertical section *pnpj-FET* structure and CMOS capacitor





2×*npn* (GC) semiconductor structure (upper)
pnpn (TW) semiconductor structure (lower)



pnpj-FET semiconductor structure

Number of available components

PNPJF (p-n-p + p-JFET)	128
GC (n-p-n + n-p-n)	128
NPNC	32
TW (n-p-n + n-p-n + p-n-p)	48
Low-noise *n-p-n*	48
Low-noise *p-JFET*	24
Dual-gate *p-JFET*	8
Total capacitance:	61.84pF/
Array/Tile	7.2pF/
Total resistance :	6.88MOm/
Array/Tile	0.86MOm

Pad frame size ~2.7x3.6 MM

Feodor Ziaziulia