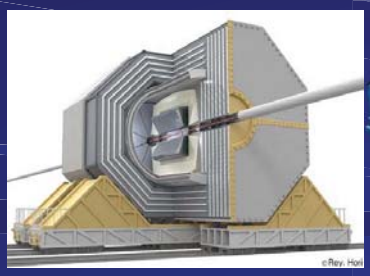
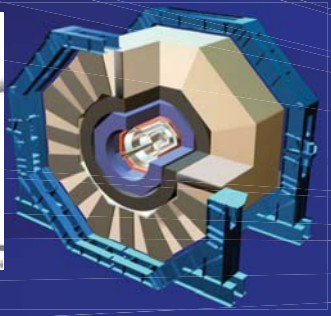
Trigger & DAQ issues for ILC
(From event selection to Physics at the future International Linear Collider)

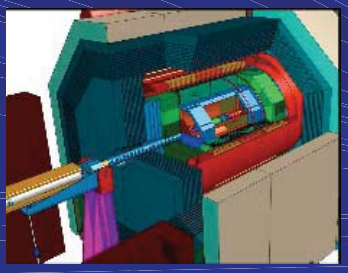
By P. Le Dû

pledu@cea.fr

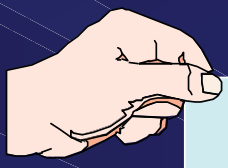
DSM - DAPNIA







?



Menu

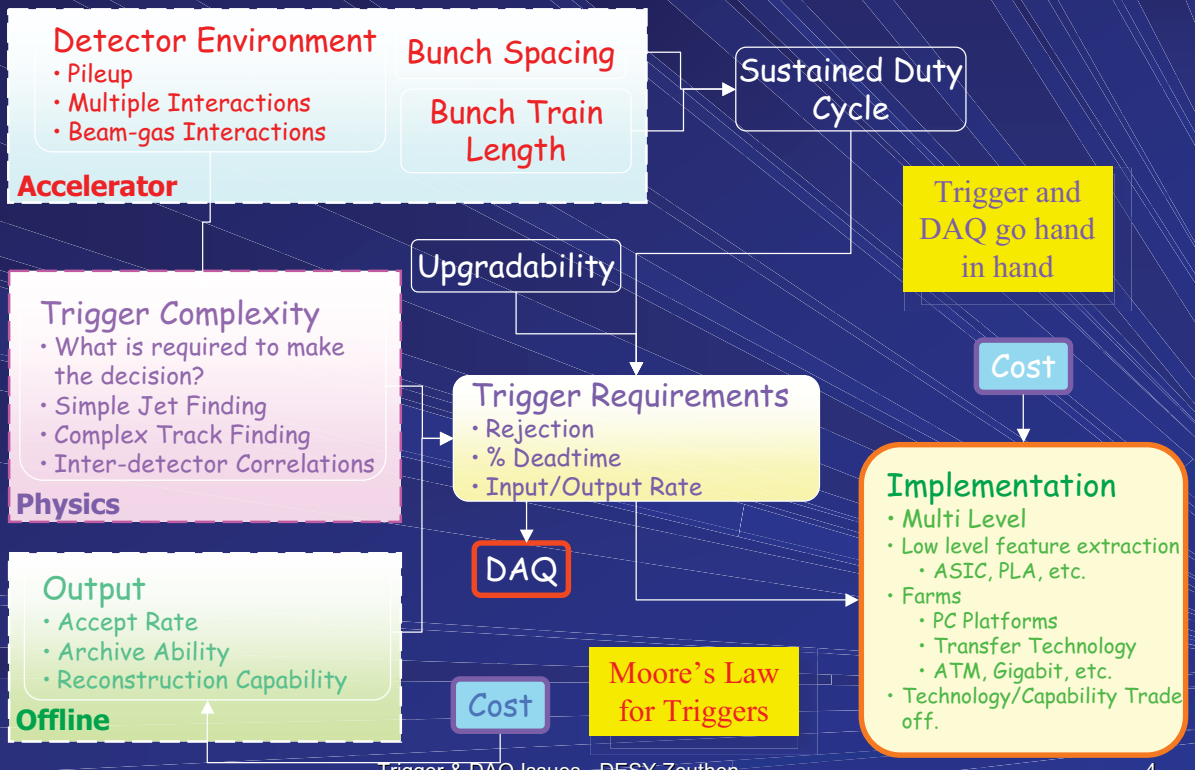
- Today Trigger & DAQ status
- Summary of present thinking
- SoftwareTrigger concept
- Data selection & collection model
- Read Out architecture
- Technology forecast
- Strategy for a future program

Goals of this presentation

Brief overview of the T/DAQ issues and directions for the future illustrated by few typical examples

- past	→ LEP (OPAL),SSC (SDC)
- present (2006)	→Tevatron (CDF,D0)
- tomorrow (2007)	→ LHC (ATLAS,CMS)
- future (> 2015)	→ ILC → GLD,,LDC,SiD …

Constraints → a multiparameters problem



Evolution of basic parameters

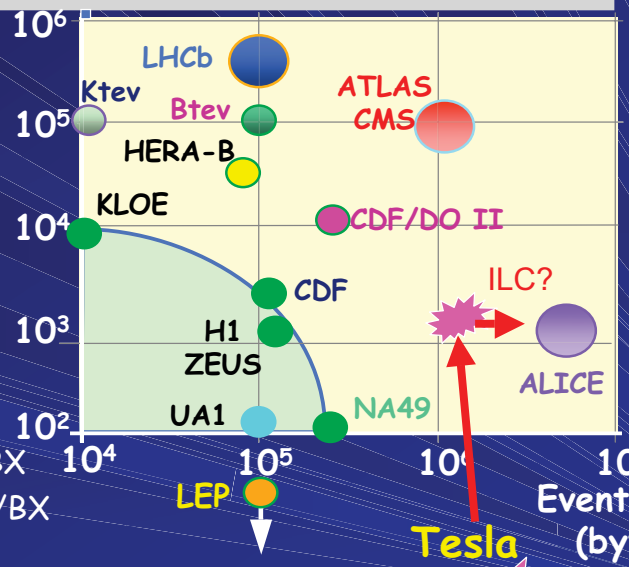
Exp. Year	Collision rate	Channel count	L1A rate	Event building	Processing. Power	Sociology
UA's 1980	3 µsec	-	-	-	5-10 MIPS	150-200
LEP 1989	10-20 µsec	250 - 500K	-	10 Mbit/sec	100 MIPS	300-500
BaBar 1999	4 ns	150K	2 KHz	400 Mbit/s	1000 MIPS	400
Tevatron 2002	396 ns	~ 800 K	10 - 50 KHz	4-10 Gbit/sec	5.10^4 MIPS	500
LHC 2007	25 ns	200 M*	100 KHz	20-500 Gbit/s	$>10^6$ MIPS	2500
ILC 2020 ?	330 ns	900 M*	3 KHz	10 Gbit/s	$\sim 10^6$ MIPS ?	> 3000 ?

* *including pixels*

Sub-Detector	LHC	ILC
Pixel	150 M	800 M
Microstrips	~ 10 M	~30 M
Fine grain trackers	~ 400 K	1,5 M
Calorimeters	200 K	30 M
Muon	~1 M	

Rates and data volume

High Level-1 Trigger
(1 MHz)



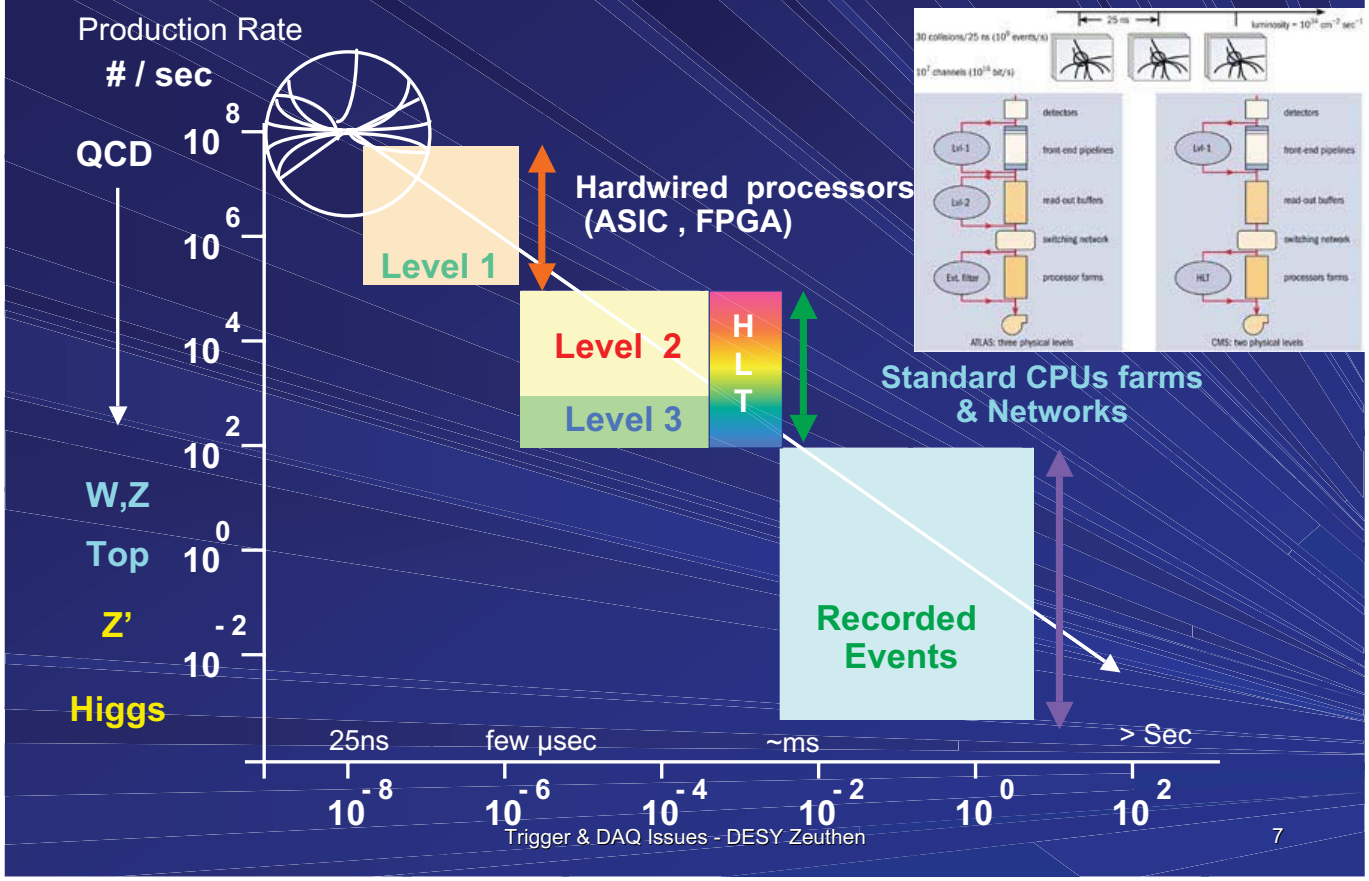
TESLA numbers

- *Physics Rate :*
  - e+ e- → X 0.0002/BX
  - e+ e- → e+ e- X 0.7/BX
- *e+ e- pair background :*
  - VXD inner layer 1000 hits/BX
  - TPC 15 tracks/BX

→ *Background is dominating the rates !*

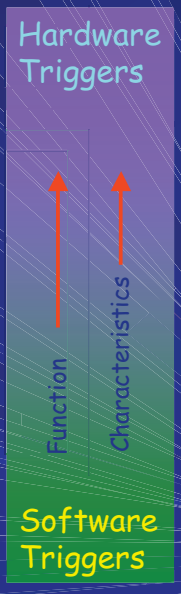
Need a new estimation for ILC

LHC Multilevels Selection scheme

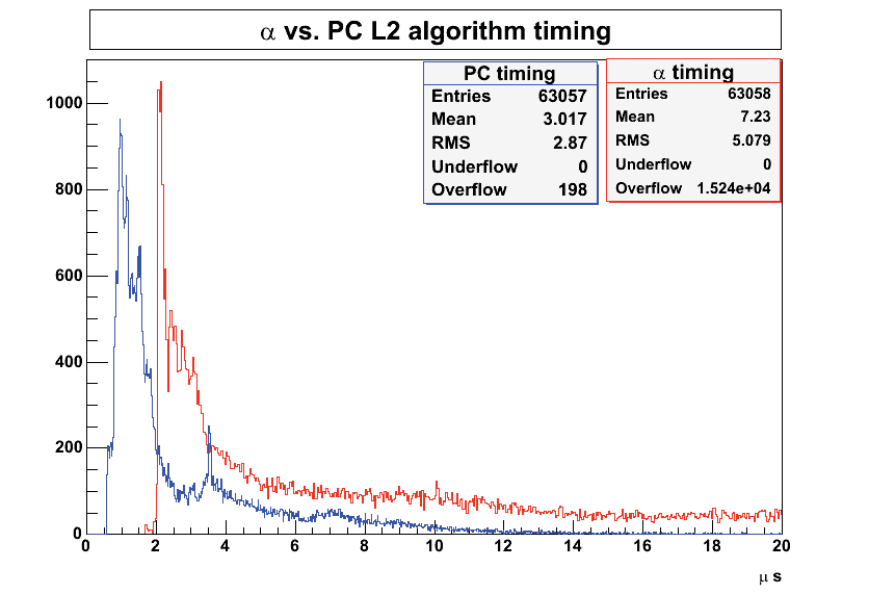


Present evolution (Tevatron,LHC ...)

- **Higher level trigger decisions are migrating to the lower levels → Software Migration is following functional migration**
  - Correlations that used to be done at Level 2 or Level 3 in are now done at Level 1.
  - More complex trigger (impact parameter!) decisions at earlier times (HLT) → Less bandwith out of detector?
- **Boundaries**
  - L2 and L3 are merging into High Levels Triggers
  - DAQ and trigger data flow are merging
  - On-line and off-line boundaries are flexible
- **Recent Developments in Electronics**
  - Line between software and hardware is blurring
  - Complex Algorithms in hardware (FPGAs)
  - Possible to have logic designs change after board layout
  - Fully commercial components for high levels.



The Tevatron (CDF) L2 lesson …..



- Alpha = many years of efforts ….hardware and software
- PC (Commercial): few months to implement! No hrdware !

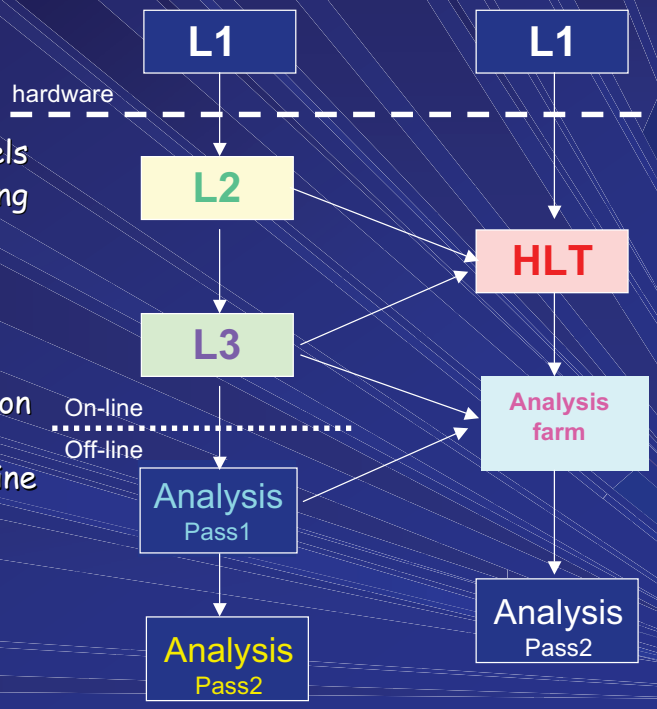
On-Off line boundaries

- **Detectors are becoming more stable and less faulty**
  - High efficiency, Low failure rate
  - Powerfull "on-line" diagnostics and error recovery (expert systems)
- **On-line computing is increasing and not doing only "data collection": More complex analysis is moving on-line**
  - "Off-line" type algorithms early in the selection chain (b tag ..)
  - Selection of "data streams" --> Important role of the "Filter"
  - Precise alignment needed for triggering
  - Detector calibration using Physics process available
  - On-line calibration and correction of data possible
- **Common aspect →**
  - Algorithms, Processing farms, Databases…
  - use similar hw/sw components (PC farms..)

Boundaries become flexible

Summary of T/DAQ architecture evolution

- Today
  - Tree structure and partitions
  - Processing farms at very highest levels
  - Trigger and DAQ dataflow are merging
- Near future
  - Data and control networks merged
  - Processing farm already at L2 (HLT)
  - More complex algorithms are moving on line
  - Boundaries between on-line and off-line are flexible
  - Comodity components at HLT



ILC machime conditions

2004 International decision: « cold » machine ' à la Tesla'

Machine parameters close to

- 2 x 16 km superconducting Linear **independant** accelerators
- Max 2 interaction points

→ **2 detectors ???**

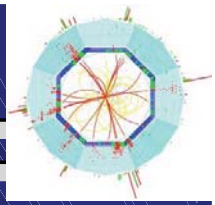
- Energy
  - nominale : 500 Gev
  - maximum : 1 Tev
- IP beam size ~ few μm
- L= 2. 10 ^{34} cm^{-1}s^{-1}

The LC is a pulsed machine

- repetitian rate 5
- bunches per train 2820 → **x 2 ?**
- bunch separation 337 ns →150ns
- train length 950 ns
- train separation 199 ms

-> long time between trains (short between pulses)

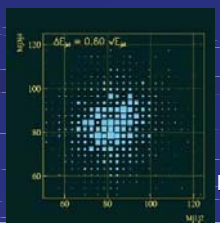
ILC vs LEP/SLD



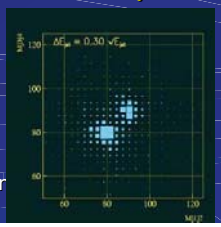
- Jets & leptons are the fundamental quanta at the ILC. They must be identified & measured well enough to discriminate between Z's, W's, H's, Top, and new states. **This requires improving jet resolution by a factor of two. Not trivial!**
- Charged Particle tracking must precisely measure 500 GeV/c (5 x LEP!) leptons for Higgs recoil studies. …. **This requires 10 x better momentum resolution than LEP/SLC detectors and 1/3 better on the Impact Paramater of SLD!**
- To catch multi-jet final states (e.g. t tbar H has 8 jets), need real 4π solid angle coverage with full detector capability. **Never been done such hermiticity & granularity!**

LEP-like resolution

$60\%\sqrt{E}$



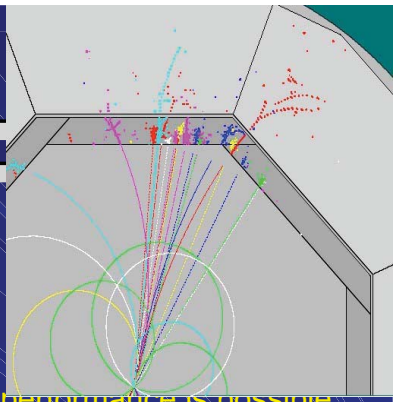
2 Jets separation



ILC goal

$30\%\sqrt{E}$

ILC vs LHC



Less demanding …..

LC Detector doesn't have to cope with multiple minimum bias events per crossing,
high rate triggering for needles in haystacks,
radiation hardness…
→ hence many more technologies available, better performance is possible.

BUT → LC Detector does have to cover full solid angle, record all the available CM energy, measure jets and charged tracks with unparalleled precision, measure beam energy and energy spread, differential luminosity, and polarization, and tag all vertices,…
→ hence better performance needed, more technology development needed.

Complementarity with LHC → discovery vs precision

The 'Particle flow' paradigm in calorimeters !
→ LC should strive to do physics with ***all*** final states.
Charged particles in jets more precisely measured in tracker
Good separation of charged and neutrals

Summary of present thinking

The ILC environment poses new challenges & opportunities which will need new technical advances in Data Collection

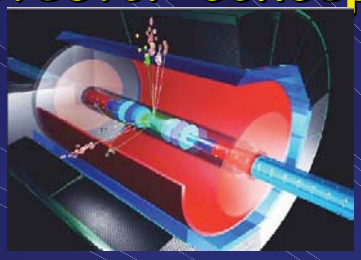
→ NOT LEP/SLD, NOT LHC !

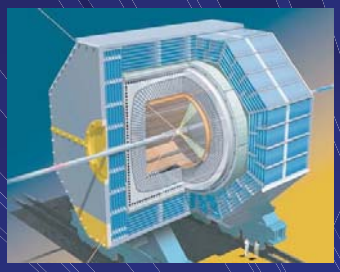
- The FEE integrates everything
  - →From signal processing & digitizer to the RO BUFFER …
- Very large number of channels to manage (Trakers & ECal)
- Interface and feedback between detector & machine is fundamental
  - →optimize the luminosity → consequence on the DAQ architecture
- Classical boundaries are moving : Slow control, On/Off line ….
- Burst mode allows a fully software trigger !
  - → Flexible, scalable and cost effective…

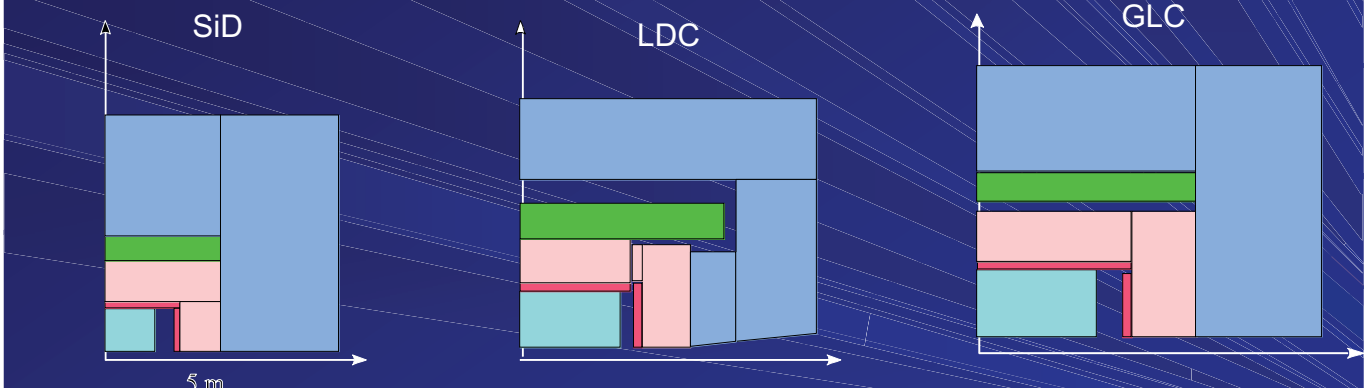
→Looks like the Ultimate Trigger: Take EVERYTHING & sort later !

→ **GREAT! A sociological simplification!**

Detector concepts



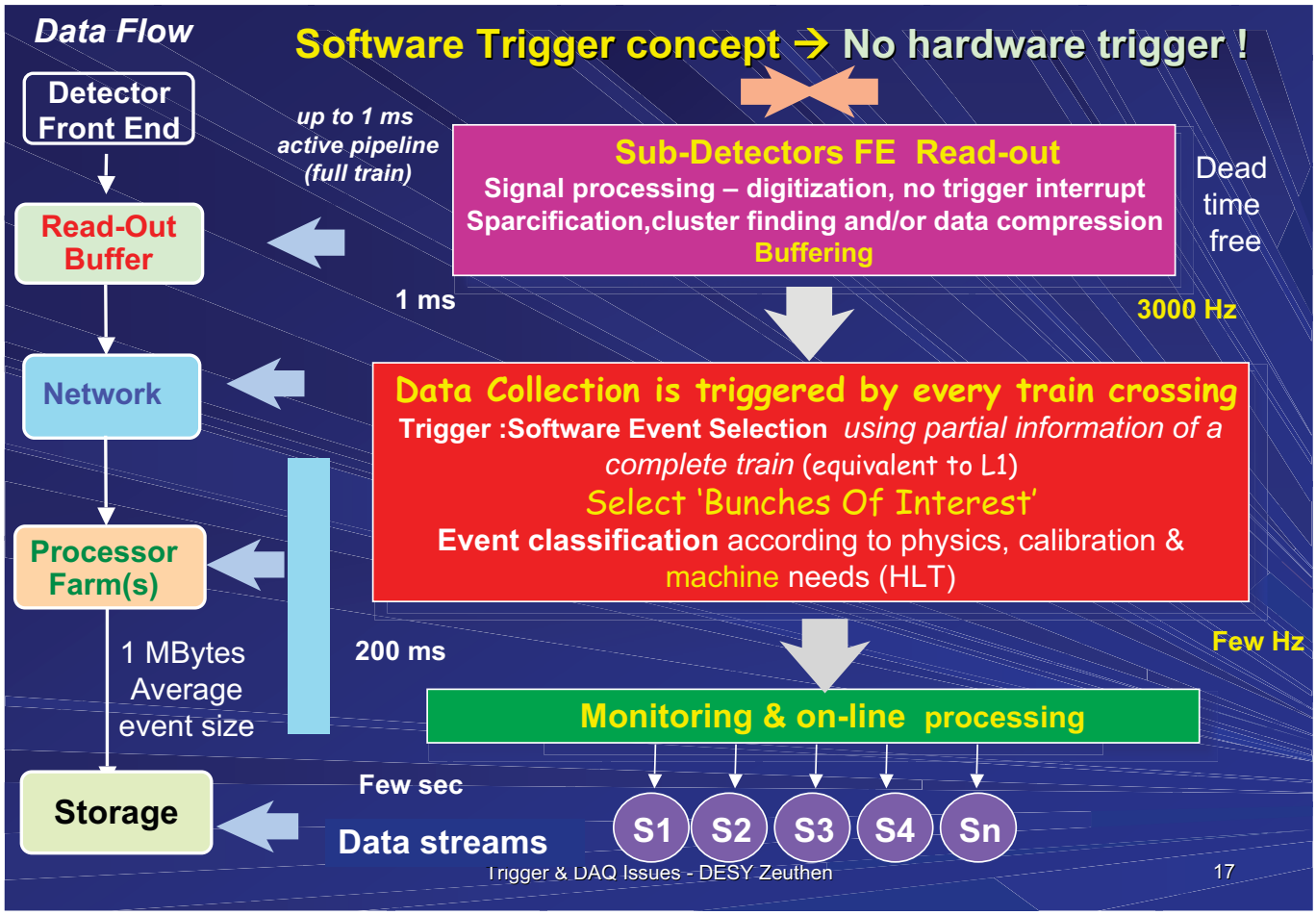


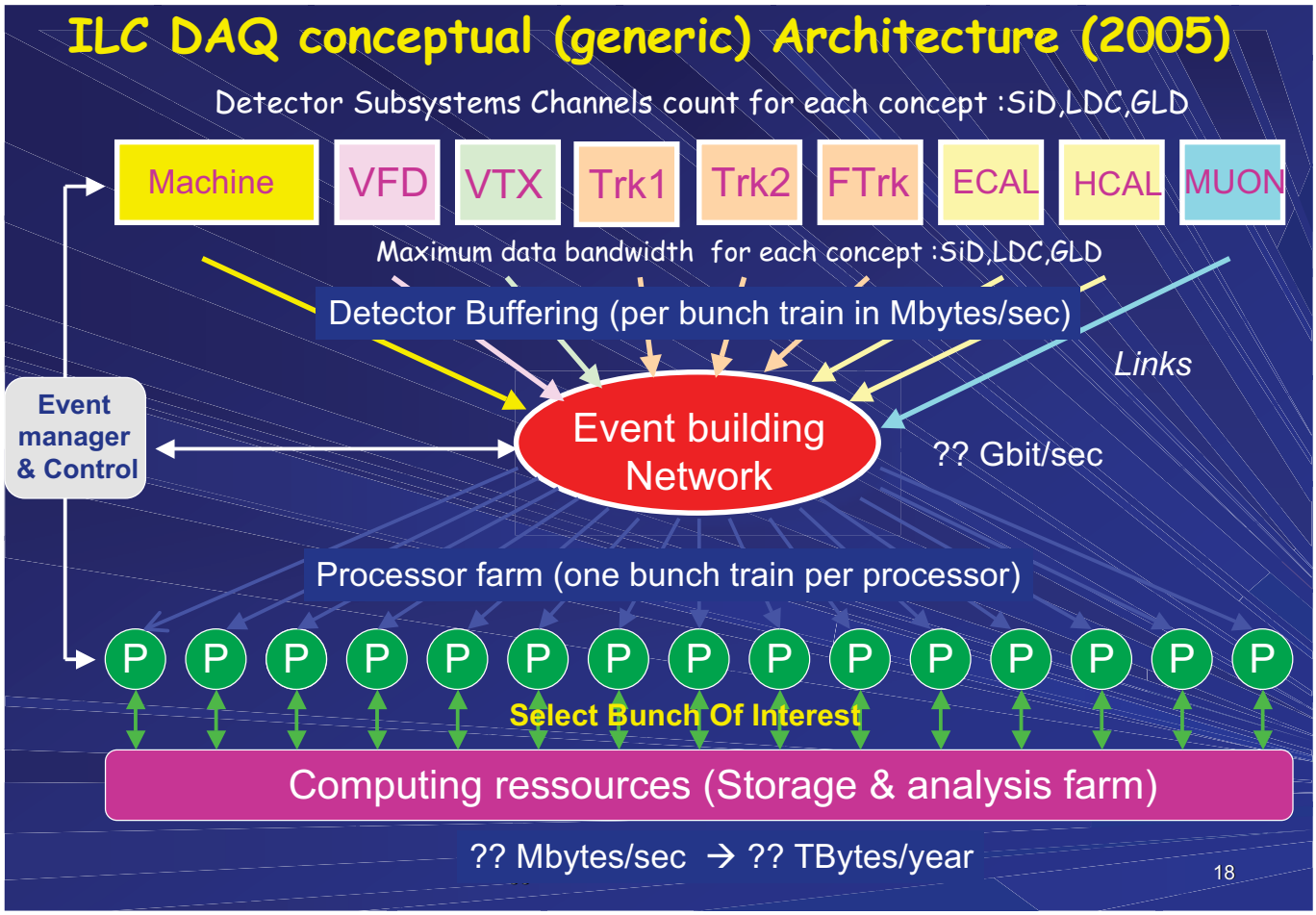


- Si Strips
- SiW EM
- 5 Teslas

- Large gaseous central tracking device (TPC)
- High granularity calorimeters
- High precision microvertex
- All inside 4T magnetic field

- Large Gazeous Tracker → TPC
- W/Scint EM calor.
- 3 Teslas solenoid


Data Flow
Software Trigger concept → No hardware trigger !
Detector Front End
Read-Out Buffer
Network
Processor Farm(s)
Storage
1 MBytes Average event size
up to 1 ms active pipeline (full train)
Sub-Detectors FE Read-out
Signal processing – digitization, no trigger interrupt
Sparcification,cluster finding and/or data compression
Buffering
Dead time free
1 ms
3000 Hz
Data Collection is triggered by every train crossing
Trigger :Software Event Selection using partial information of a complete train (equivalent to L1)
Select 'Bunches Of Interest'
Event classification according to physics, calibration & machine needs (HLT)
200 ms
Few Hz
Monitoring & on-line processing
Few sec
Data streams
S1
S2
S3
S4
Sn
Trigger & DAQ Issues - DESY Zeuthen
17


ILC DAQ conceptual (generic) Architecture (2005)
Detector Subsystems Channels count for each concept :SiD,LDC,GLD
Machine
VFD
VTX
Trk1
Trk2
FTrk
ECAL
HCAL
MUON
Maximum data bandwidth for each concept :SiD,LDC,GLD
Detector Buffering (per bunch train in Mbytes/sec)
Links
Event manager & Control
Event building Network
?? Gbit/sec
Processor farm (one bunch train per processor)
P
Select Bunch Of Interest
Computing ressources (Storage & analysis farm)
?? Mbytes/sec → ?? TBytes/year
18

About systems boundaries …..moving due to !
→ evolution of technologies, sociology ……

NEW !

Machine
Synchronization
Detector feedback
Beam BT adjustment

Subdetectors
FE Read Out
Signal processing
Local FE Buffer

Uniform interface

Full Integration of Machine DAQ In the data collection system

Read out Node
Partitionning (physical and logical)

Data Collection (ex on-line)
Bunch Train data collection from Buffer RO
Bunch Of Interest selection
SW trigger & algorithms
Event Building
Control - supervisor
On line Processing
Global calibration ,monitoring and physics
Local (temporary) Data logging (Disks)

Global Detector Network (worlwide)
- Detector Integration
- Remote Control Rooms (3?)
  - Running modes
    - Local stand alone
    - Test
    - Global RUN
  - Remote shifts
    - Slow control
    - Detector Monitoring
- Physics & data analysis (ex On- Off line)
  - Farms
  - GRID …
- Final Data storage

Current view of a uniform RO architecture

Sensor technology

Integration
To be studied!

Common/uniform Interface

Local/Global Controls & Services
Partition
Running mode (Stand alone, test, RUN)
Synchronization & machine interface
Databases : Calibration & Monitoring ……

VTX
CCD
MAPS
DEPFET
…..
TRK
Si
TPC
ECAL
Si W
Scint W
HCAL
Digital
Analog
Muon
RPC
Scint …
VFD

On detector Very Front End

Preampli Shaper Digitizer

Local Signal Processing and buffer

Front End (On / Near detector)

FPGA

Local Data Management

G D N

Global Detector Network

Receiver
Digital Processing
MUX
RO Buffer

Read Out Node/Hub

Dedicated ASIC and/or SOC*

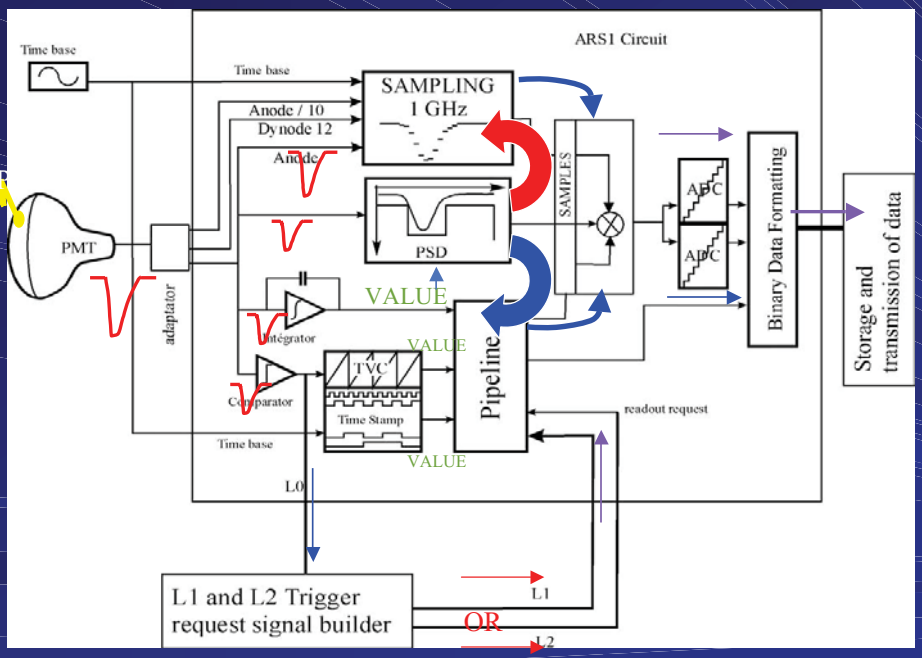
Commercial standard

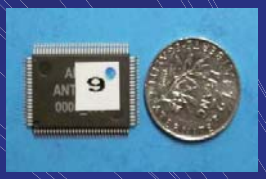
*System On Chip

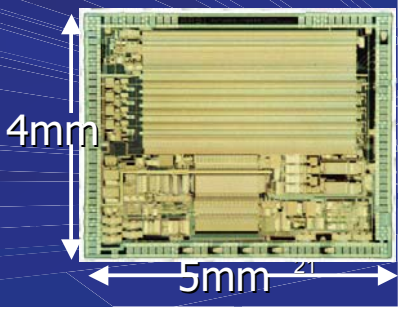
Toward SOC (System On Chip)

[E. Delagnes CEA-Saclay]

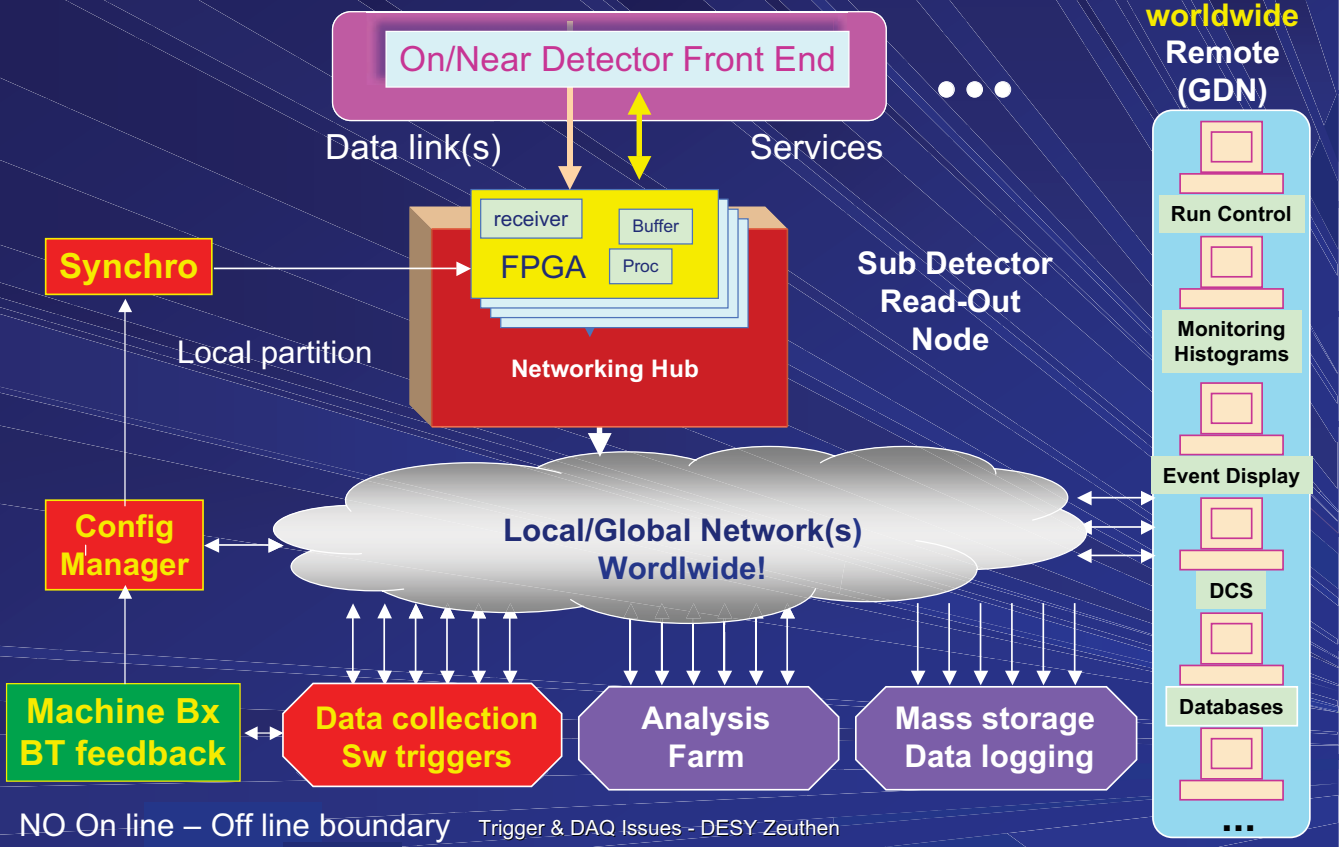
- System on Chip : several functions integrated
  - Ex : Front-end chip for Antarès : pipelines 1GHz, TDC, ADCs…



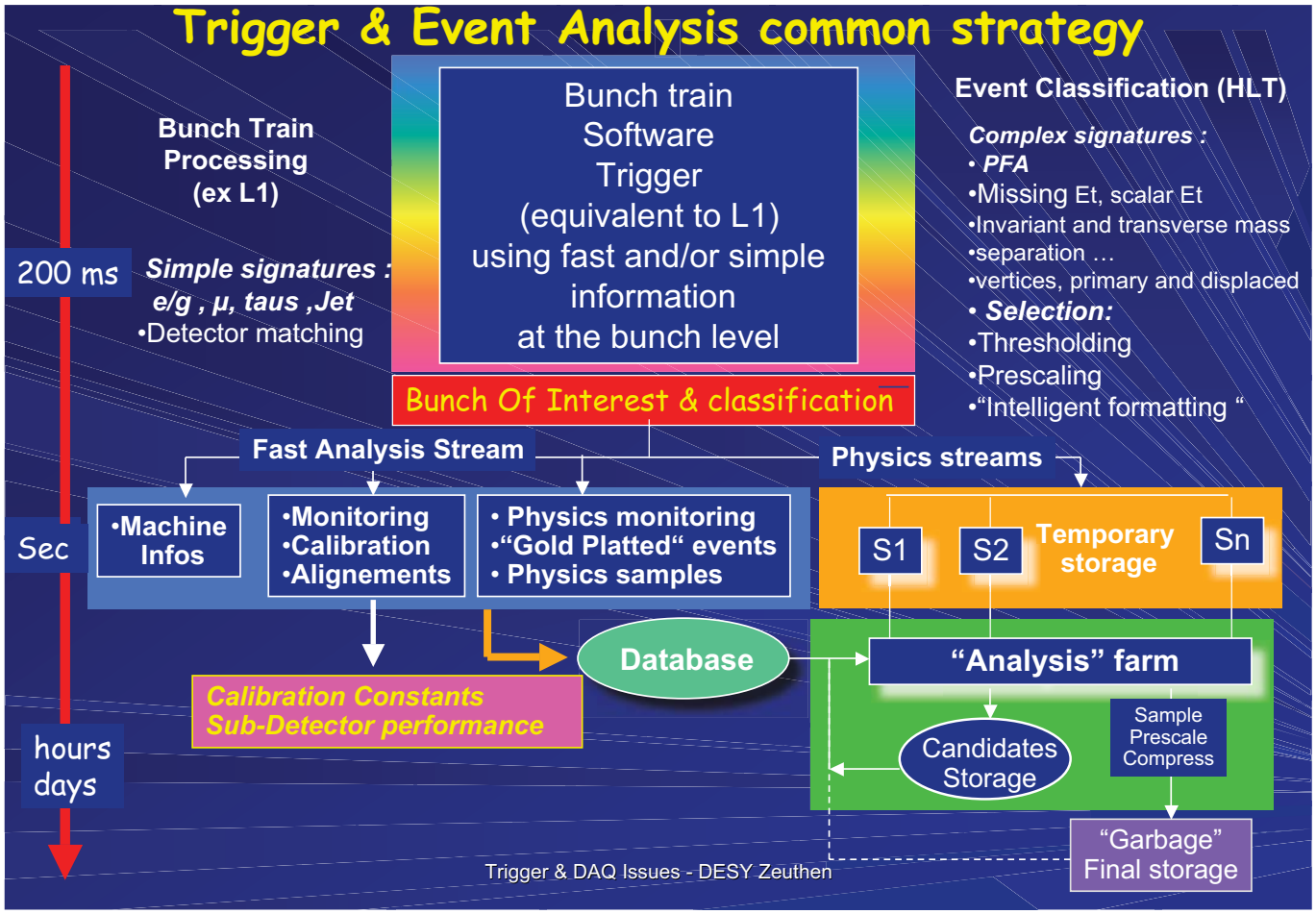




ILC 'today' Data Collection Network model



Trigger & Event Analysis common strategy



Strategy for event selection @ LHC

40 MHz

L1

100 KHz

L2

1 KHz

L3

100 Hz

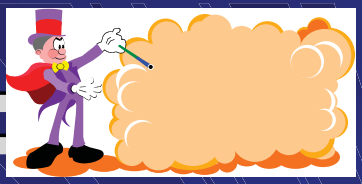
- **"Local" identification of high Pt objects → *use coarse dedicated data***
  - Electrons /Photons , Hadrons & Jets → Energy clusters
  - Muons → Track segments
  - Neutrinos → Missing Et
- **Particle signature (e/g,h,Jet, μ ...) → *use final digitized data***
  - Refine Pt cuts → fine granularity & track reconstruction
  - Combine detectors → Converted electron ,"Punchthrough", decays
- **Global topology** → multiplicity & thresholds
- **Identification & classification of physics process → trigger menu**
  - Partial event reconstruction → Vertices , Masses ,Missing Et....
- **Physics analysis**
  - "Off-line" type analysis of classified events

Technology forecast

Summary of the talk given by D. Calvet at the IEEE Real Time Conference ;Stockholm 4-10 june 2005.
"A Review of Techniques and Technologies for the Transport of Digital Data in Physics Experiments"

- **End of traditional parallel backplane bus paradigm**
  - Announced every year since ~1989
  - VME-PCI still there; watch PCI Express, RapidIO, ATCA
- **Commercial networking products for T/DAQ**
  - DAQ 94' Conferences: ATM, DS-Link, Fibre Channel, SCI
  - Today: Gigabit Ethernet (1 → 10 → 30 GB/s)
- **The ideal processing / memory / IO bandwidth device**
  - The past: Transputers, DSP's, RISC processors
  - Today: FPGA's → Integrates receiver links, PPC, DSP's and memory ….

Technology forecast (Con't)



- **Point-to-point link technology**
  - The old style: Parallel Copper – Serial Optical
  - The modern style: Serial Copper – Parallel Optics
    - >3Gb/s today, 10Gb/s in demonstration
- **Processors** → Moore's law still true until 2010 ….at least !
  - Continuous increasing of the computing power
  - Today 4GHz clock → 10 to 15 GHz in 2010 !
- **Memory size → quasi illimited !**
  - Today : 256 MB
  - 2010 : > 1 GB … then ?
- **Modern wisdom (about technology)**
  - *"People tend to overestimate what can be done in one year, and underestimate what can be done in 10 years."*

The LHC example

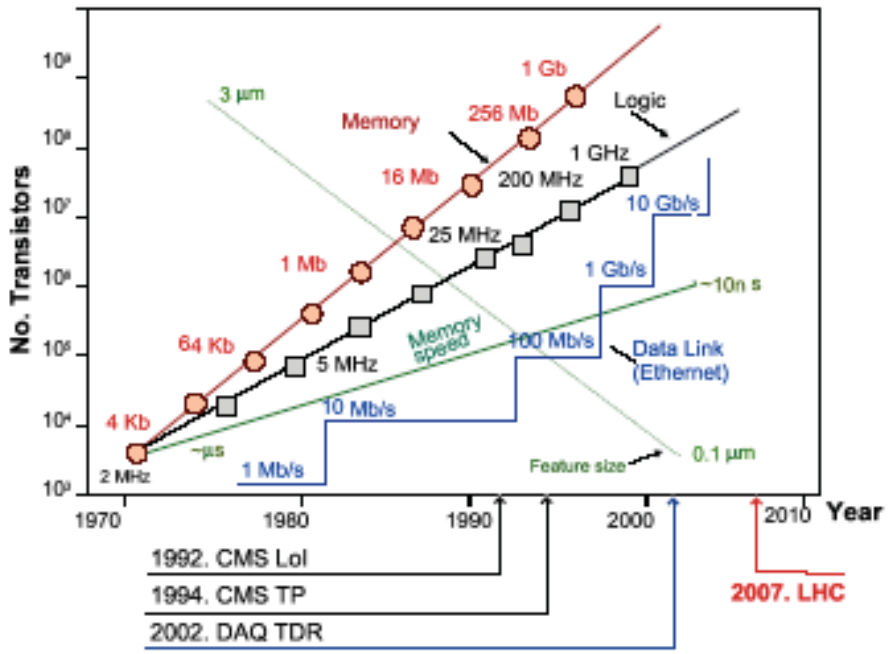


Table 1: I/O Bus Bandwidth Comparison

	I/O Bus	MHz	Bus Width Bits	Rate Mbytes/sec	Transmission	Measured @ Yale
PC Buses	Industry Standard Architecture (ISA)	8.3	16	8.3		
	Extended Industry Standard Architecture (EISA)	8.3	32	33		
	Peripheral Component Interconnect (PCI)	33	32	132		
	AGP4X			1,000		
	AGP8X			2,000		
Networks	Ethernet	10	1	1.25	CAT 5 Cable	
	USB 2.0	480 mb	1	55		40
Networks	Gigabit Ethernet	1250	1	125	CAT 5 Cable	65%
	PCI Express	2500	x1	250	Dual Simplex	
			x4	1,000	Dual Simplex	
	PCI Express Gen2	5000	x1	500	Dual Simplex	
			x4	2,000	Dual Simplex	
Networks	Infiniband	2500	x4	1,000	Dual Simplex	75%
Instrumentation						
	CAMAC	1	24	3		3
	FASTCAMAC Level 1	2.5	24	7.5		7.5
	FASTCAMAC Level 2	10	24/48	30/60		40
	VME	10	16-64	20-80 ??		
	Compact PCI	33	32	132		

Current Working program (1) → LCWS06

- **Understanding in details Detectors Read Out schemes**
  - Establish a stable network of contacts at the Detector level
  - By Subdetectors technologies→ Independently of detector concepts
  - By Detector concepts SiD,LDC,GLD → what are the particularities?
  - Propose a uniform architecture (VTX,TRK, CALORs,Muon …)
    - Do not forget the Very Forward !
  - Influence of technical aspects → Power cycling & beam RF pick-up ….
- **Refine the s/w trigger concept → ILC T/DAQ model**
  - Special triggers (Calibration,Tests, Cosmics …)
  - Possible Scenarios for Bunch Of Interest fast selection
    - Needs for hardware PREprocessing ?
- **Interface with machine**
  - Common aspects : can the machine & Detector DAQ should be similar?
  - Which infos and are needed?
  - Integration of Bunch Train feedback

Curent working program (2)

- **Define clearly the 'boundaries' → functional block diagram**
  - Integration of GDN → Integrated computing model (watch GRID!)
  - 'Slow controls' , monitoring , calibrations ……..
  - Partitionning …..
- **Milestones for 2006 (CDR) → Baseline ILC support document**
  - Define a list of technical issues and challenges to be addressed
  - Investigate commercial « new » tools & standards (FPGAs, ACTA, PCIexpress ,wireless? …)
- **Toward a realistic costing model**
  - Global to the 3 detectors concepts
  - Table of parameters: estimate number of channels, bandwidth ….
  - Estimate quantity of hardware (interfaces, processors, links …), software ? and manpower (is LHC a good model ? -- » 20 M Euros)

Current working program (3) → LCWS06

- **Build a wordwide 'long term' strong & stable team**
  - Seniors with experience coming from LEP/SLD,Hera/LHC/Tevatron,Babar/Belle/KEK experiments .....
  - Younger physicists and engineers with enthousiasm!
  - Establish list of contact persons for each detector/concept/machine.....
  - Include long term sociology → NOT reinventing the wheel!
    - Build ONLY what is needed ! Not competing with industry! ....
    - Do not follow the LHC exemples !
- **Define a realistic ' PILOT PROJECT ' for 2006 -2008**
  - Practicing state of the art technologies
  - Common to all the concepts and detectors R&D
  - Learning and educating process..... worldwide

Investigate the NEXT standard
→ After CAMAC, Fastbus,VME → PCI express + ATCA

ATCA in one page

(Advanced Telecommunications Computing Architecture)

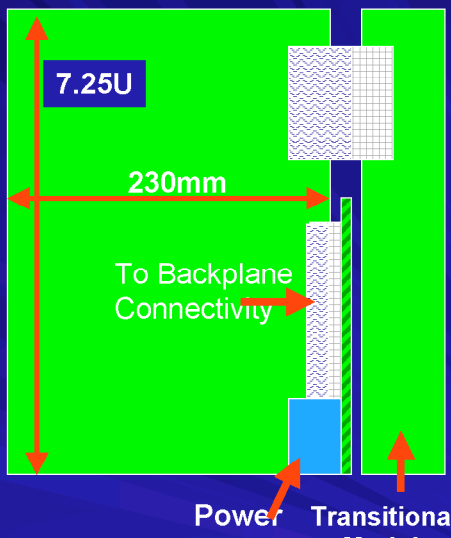
Courtesy of R.Larsen (SLAC), R.Downing (FNAL), S.Dahwan (Yale), B.Martin (CERN)

- **Coming from Telecom industry** *ITER, AGATA*
  - System throughput to 2 Tb/s
  - System Availability 99.999% (~5 min/yr)
  - Sponsored by the PIC Industrial Computer Manufacturers Group (PICMG)
- **Basics elements and features**
  - Crate & subrack (Shelf) : Backplane, Shelf Manager,Air Cooling,Power, Entry Modules
    - "Shelf Manager" manages all module, crate, system utilities
  - Module /Board (Blade) 14 to 16 units 8U .!,2 inch x 280 mm - 200W, vertical/horizontal
  - Backplane : redundant dual star and full mesh (point to point)
    - Multiprotocols : Ethernet,Fiber channel, PCI express, Infiniband, rapidIO ....
    - Synchronization and Clock Interfaces buses (6)
  - Rear Transition Module for user up 20 W
  - Carrier (Daughter Card, Plug-in Module, Advanced Mezzanine Card)
  - Software (Linux based)

Compare ATCA* & Bus systems

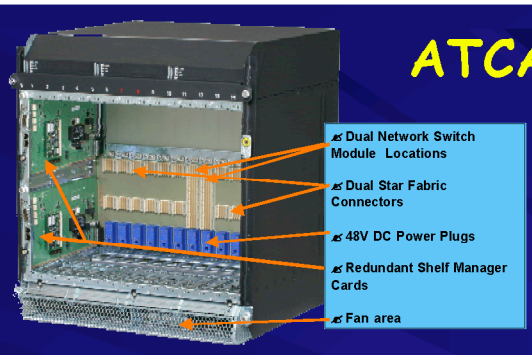
*Advance Telecom Computing Architecture

	ATCA	PCI Long	VME (6U)
Board Area cm^2	995	316	373
Power Watts	200	10/25	30
Bandwidth I/O Gb/s	20 Full Duplex	4.3 66 Mhz 64 bits	2.4 VME 2eSST
Front Panel H*W cm	30 * 23	8 * 1.2	21.5 * 23
Component height mm	21.33	14.48	13.72



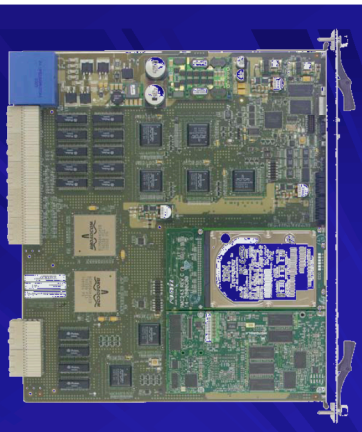
- Passive Back Plane
- - 48 Volt Power in
- Specifications for PCIe, Infiniband, GigE using the same Back plane
  - AMC (Advanced mezzanine Card)
  - mTCA based on ATC specifications - 4 U PCB
  - Interconnections for Servers

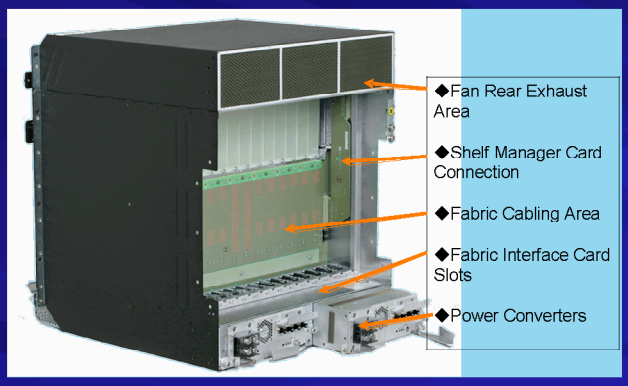
ATCA elements



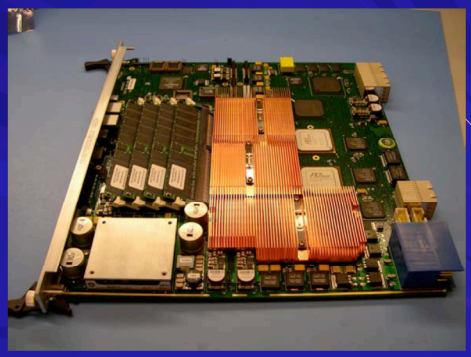
Shelf front

System Controller and Switch Blade





Shelf rear



System processor

Basic components PILOT PROJECT

Front

Rear

DETECTOR

FEE

Links

Uniform Read Out Mezannine

Advance Mezzanine Card (PCI express)

GDN

Global Detector Network

Pixel
SiLC
TPC
Calice
EUDET ….
Machine elements …

Conclusions

- A lot of exciting things to investigate
  - From physics
    - Algorithms and selection strategy
  - To state of the art NEW technologies
  - Plus an interesting sociological environment

Thanks a lot for your attention and your invitation !