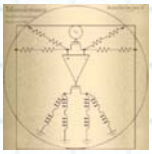

ASIC development for BeamCal

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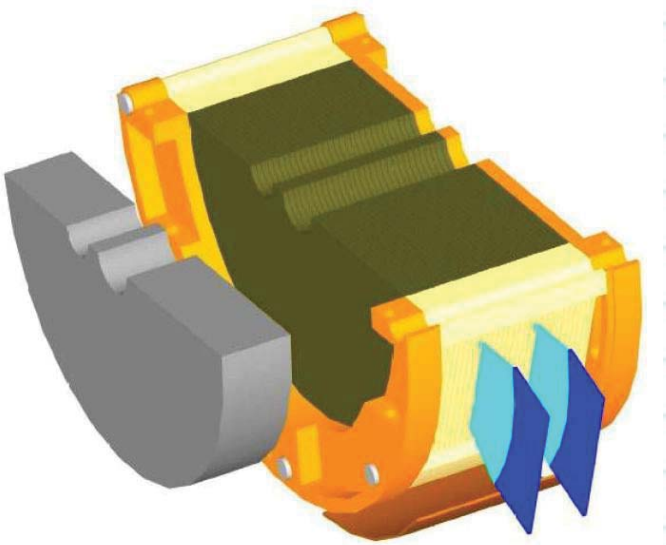
FCAL Workshop 2012 – DESY, Zeuthen
May 9, 10:15 – 10:55

Outline

- Context
- Previous work @ SLAC
- Testing @ DESY (right now!!!)
- Current research @ PUC
- Publications

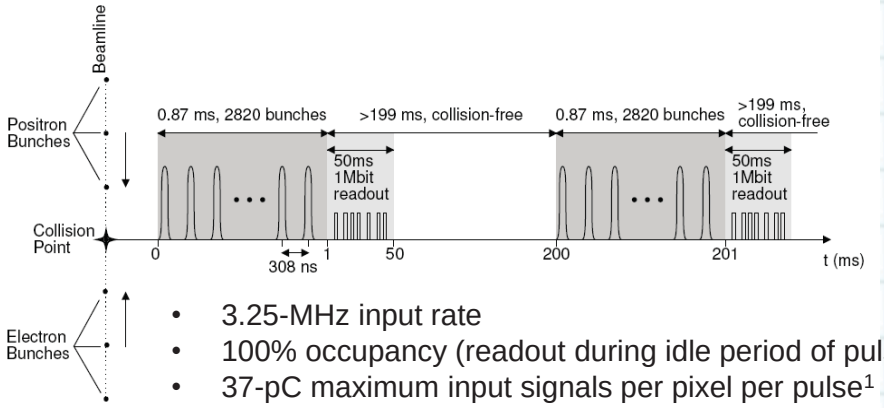
Context: BeamCal Calorimeter

- 30 layers, 45360 pixels per side
- BeamCal mission:
  - To extend the calorimeter to small polar angles
  - To reduce backscattering from pairs into the detector center
  - To provide a low latency output for beam tuning



http://www-zeuthen.desy.de/ILC/fcal/

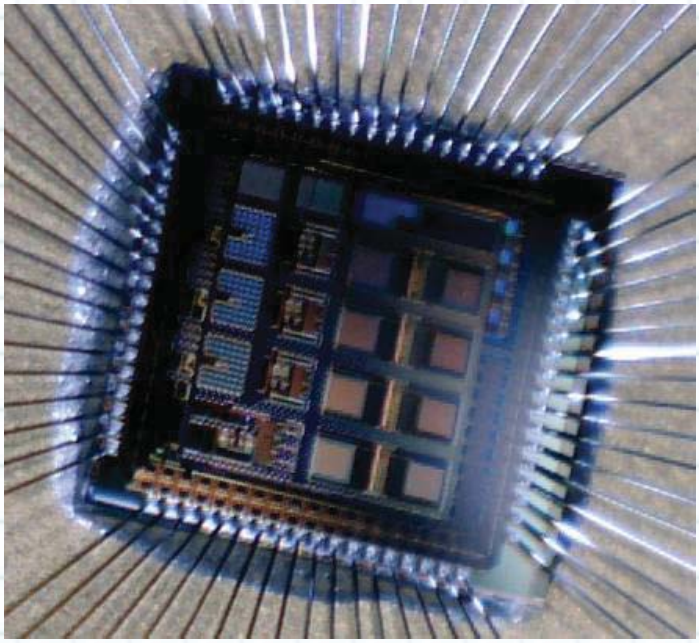
BeamCal ASIC Specifications (?)



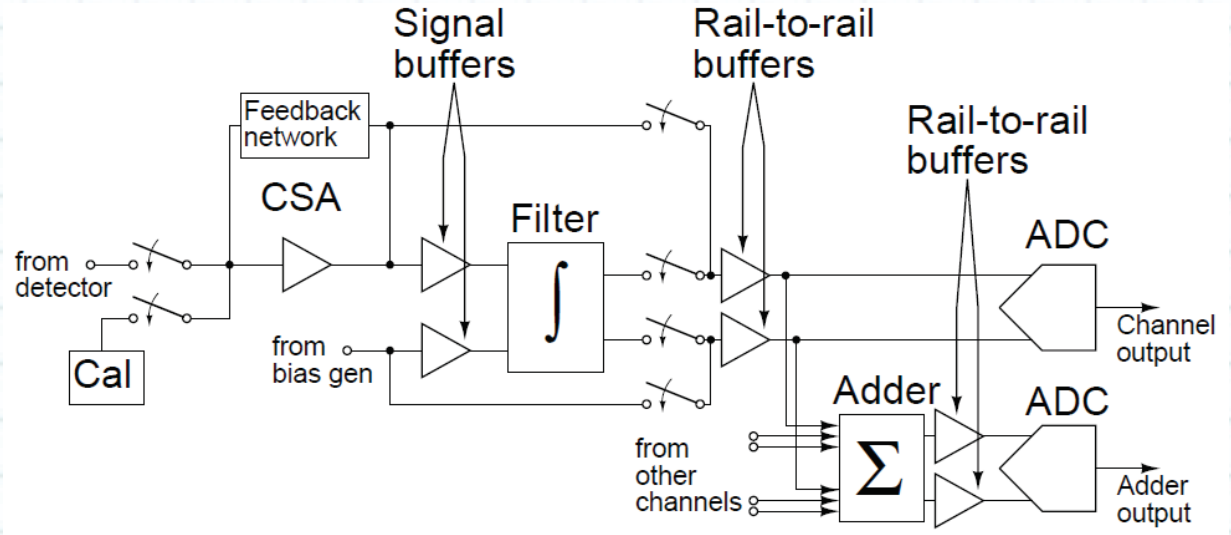
- 3.25-MHz input rate
- 100% occupancy (readout during idle period of pulse trains)
- 37-pC maximum input signals per pixel per pulse[1]
- 40-pF input capacitance
- 10-bit resolution
- Dual gain (50x) for different modes of operation: standard data taking (SDT) and detector calibration (DCal)
  - SDT: large input signal; slew rate, bandwidth and adder challenges
  - DCal: smaller input signal; noise, baseline restoration and linearity challenges (tighter design space)
- 32 channels per chip
- Full-chip output (8-bit, 1-μs latency) for beam diagnostics
- Radiation tolerance to 1 Mrad total dose

Previous work @ SLAC

- The Bean Chip V1.0
  - Taped out in November 2009
  - Tested at SLAC between March & June, 2010
  - A few kind-of-new ideas were implemented:
    - ADC with very small capacitors
    - Slow reset-release
    - SC integrator

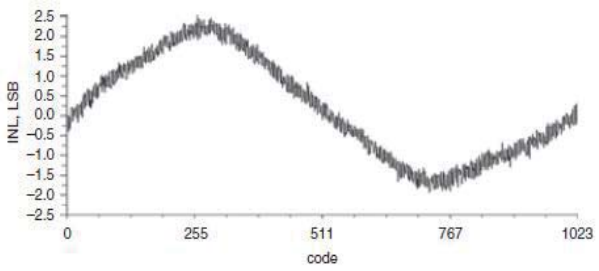


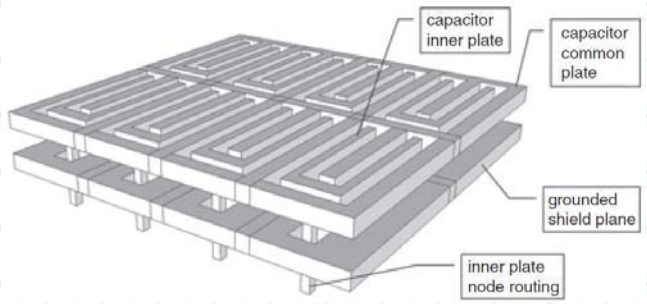
The Bean block diagram, single channel

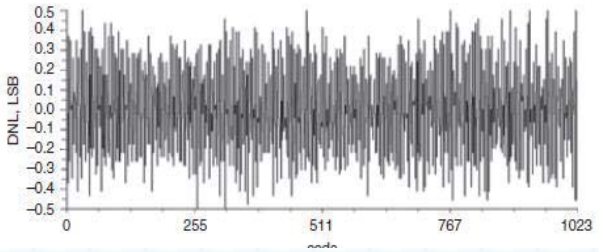


ADC with small capacitors

- 2-fF unit capacitors
- Mismatch below 10%
- Low power consumption
- Small load on driving net



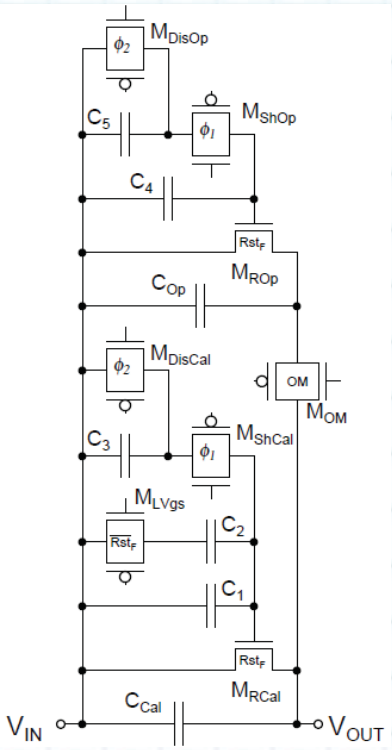




[Abusleme et al, IET Electronics Letters 2012]

Slow reset-release technique

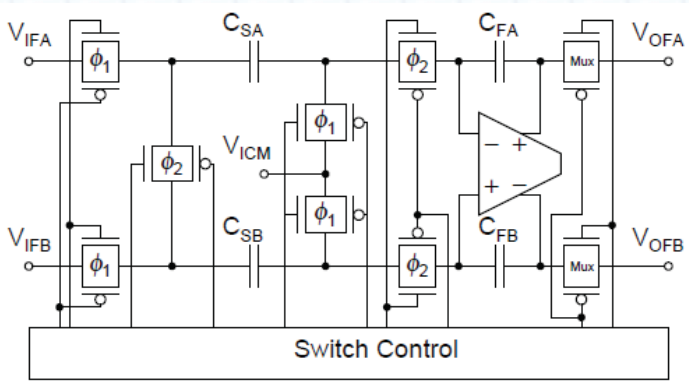
- Acts on charge amplifier (CSA) feedback network
  - Allowing to release the reset action slowly
  - Not as effective as CDS, but simpler
  - Requires less CSA integrating time than CDS
    - Adequate when parallel noise is an issue
  - Allows higher certainty on the output swing

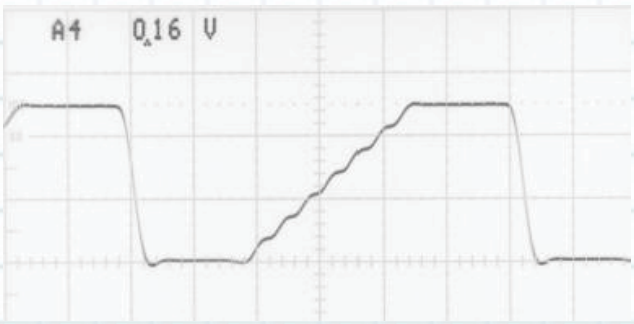


[Abusleme et al, IEEE TNS, 2012]

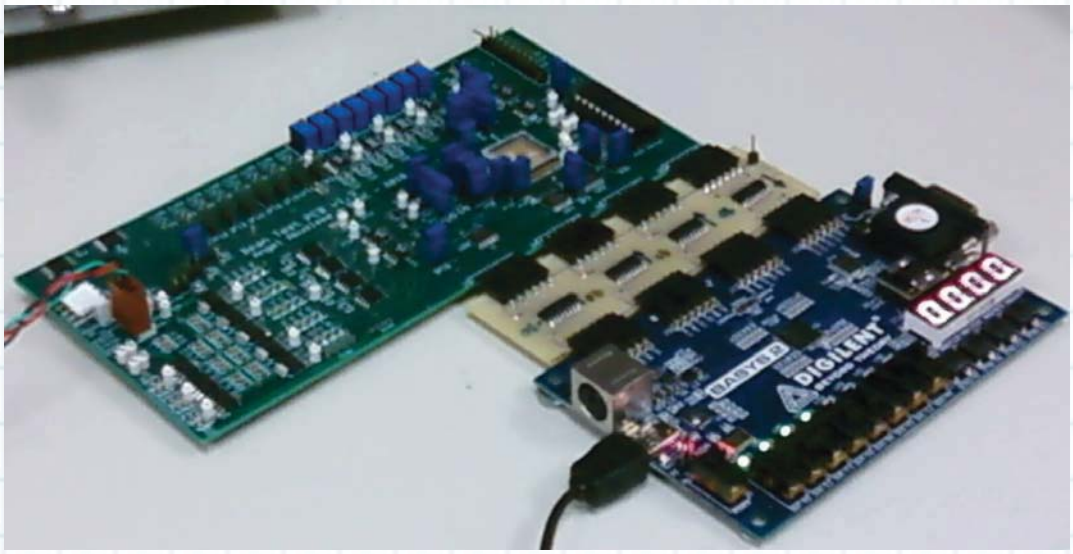
SC integrator

- An analog filter in the discrete-time domain
- Not as effective as a continuous-time filter, but
  - Compatible with standard CMOS processes
  - Time constants are defined precisely
  - It allows a wide range of programmability
    - E.g., to generate arbitrary weighting functions



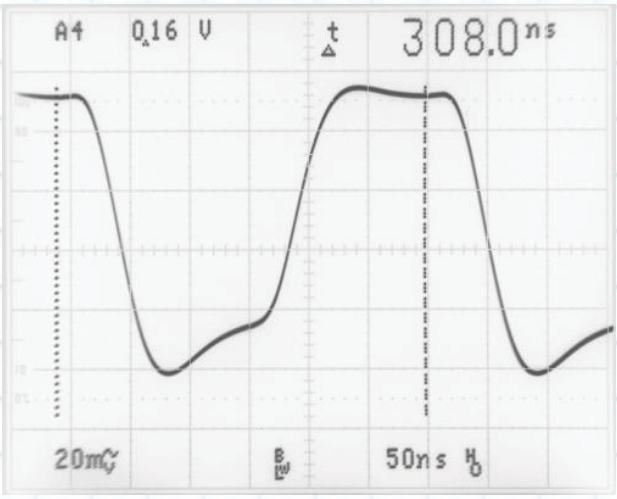


Tests @ SLAC

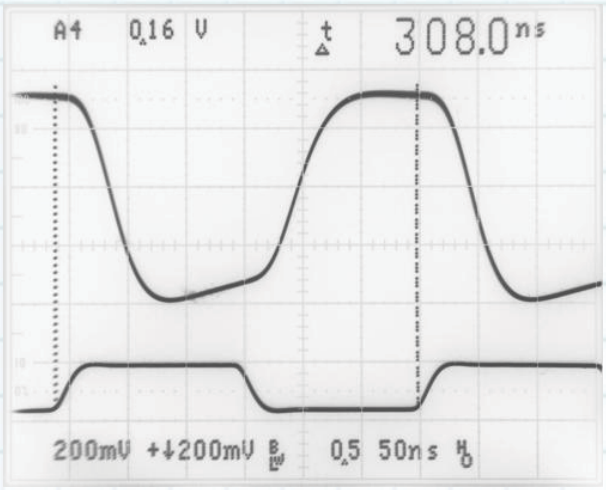


CSA operation

CSA Output, standard data taking
Nominal speed

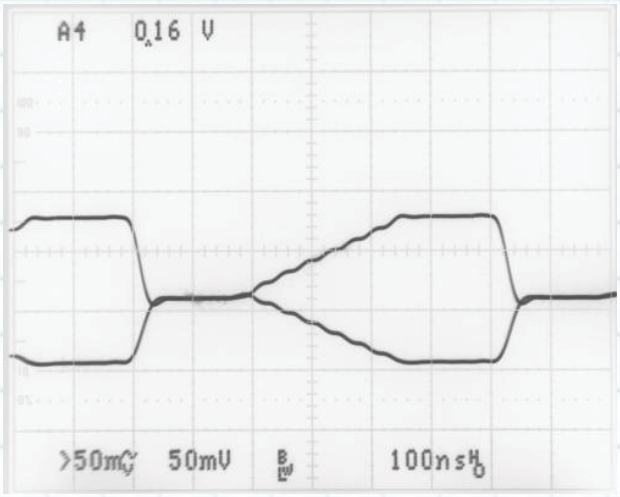


CSA Output and reset signal,
Calibration mode,
Nominal speed

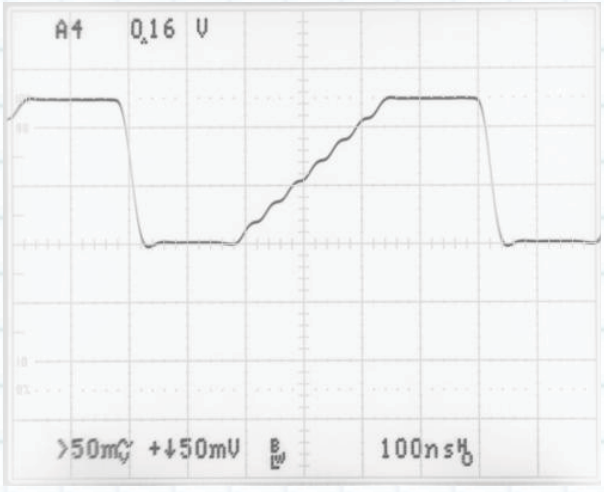


Filter operation

Filter output, single ended
½ speed

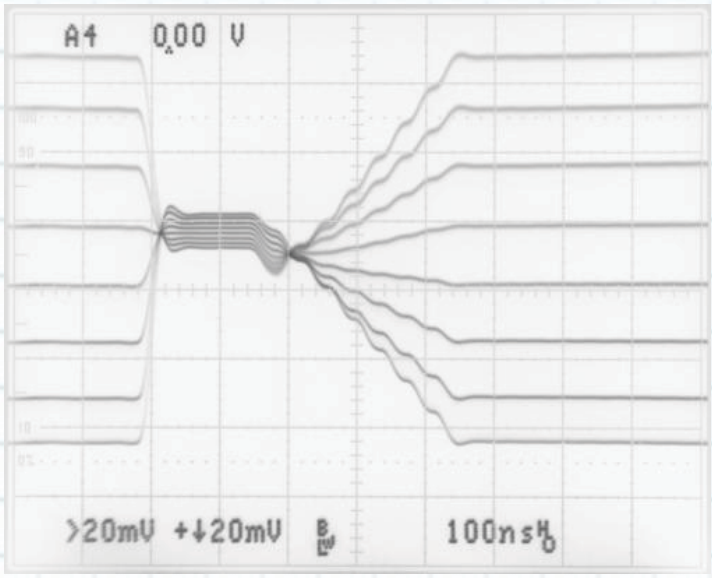


Filter output, fully differential
½ speed



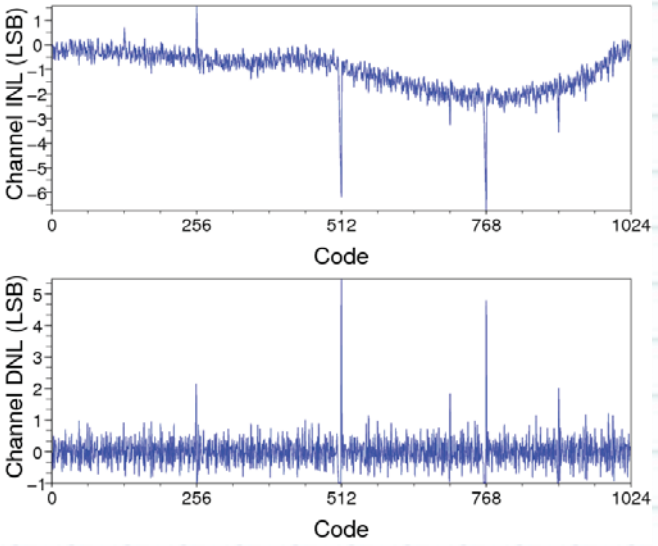
More on filter operation

Filter output for input charge sweep, ½ speed

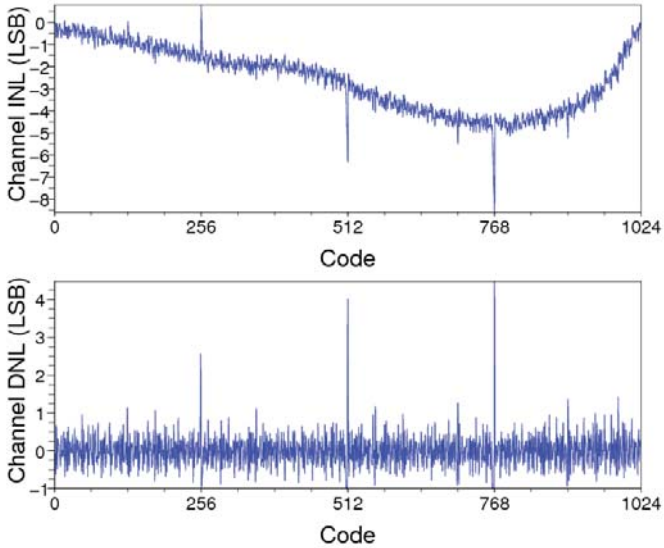


Linearity, SDT mode

37 pC input

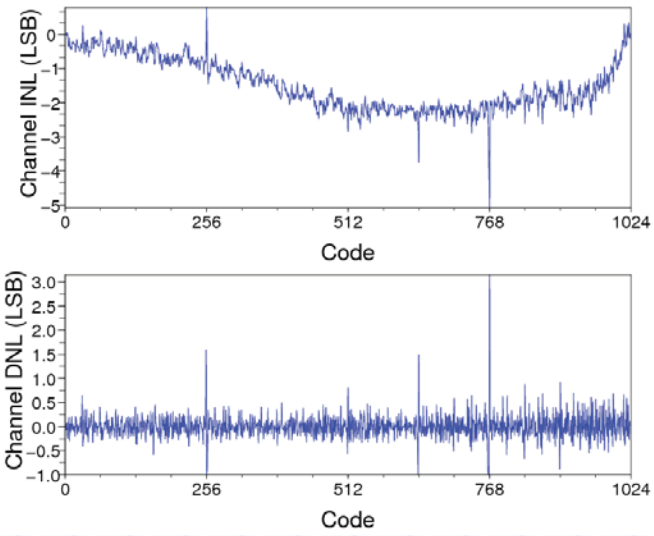


40 pC input

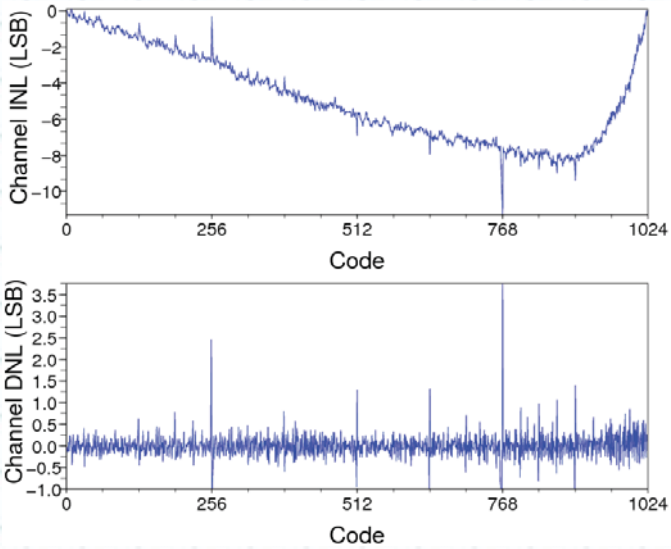


Linearity, DCal mode

0.74 pC input

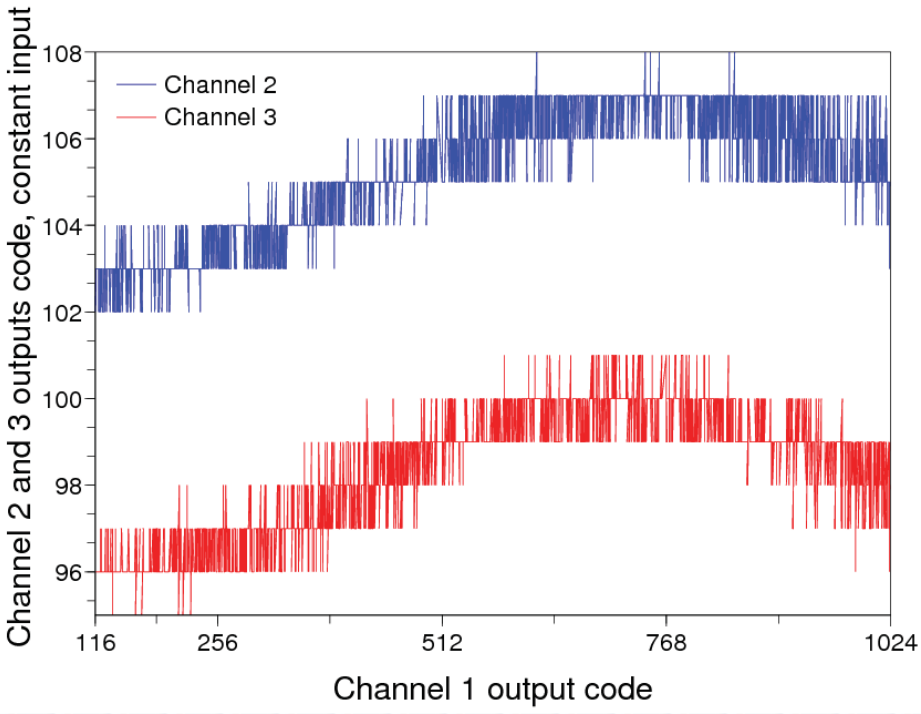


0.86 pC input



Crosstalk, SDT mode

- Ramp input in Ch01
- 4096 values recorded on Ch02 and Ch03
- Nominal speed



Crosstalk, DCal mode

- Ramp input in Ch01
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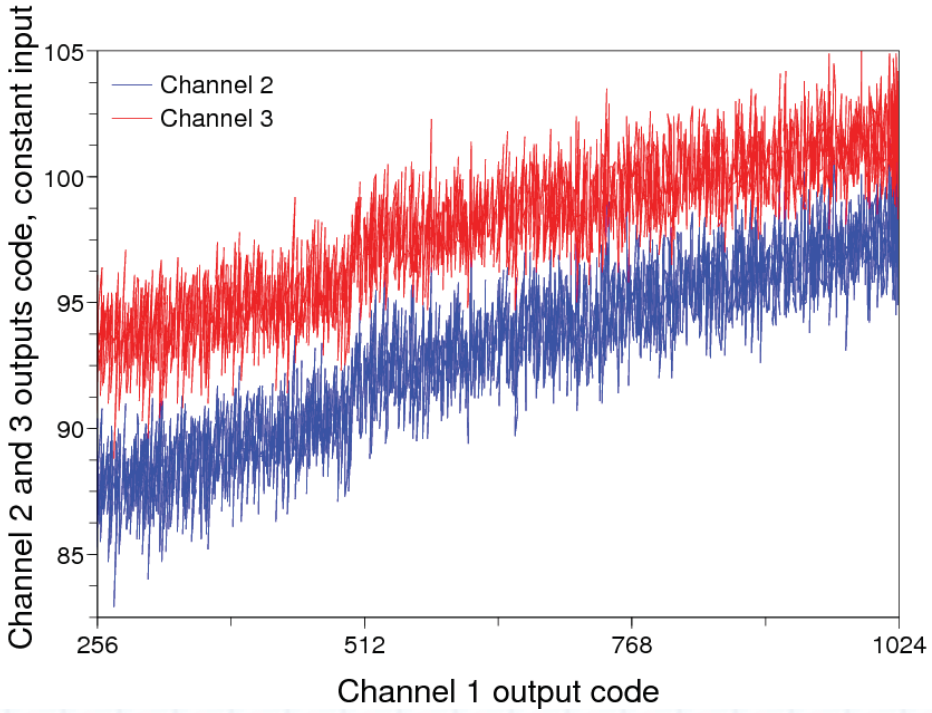
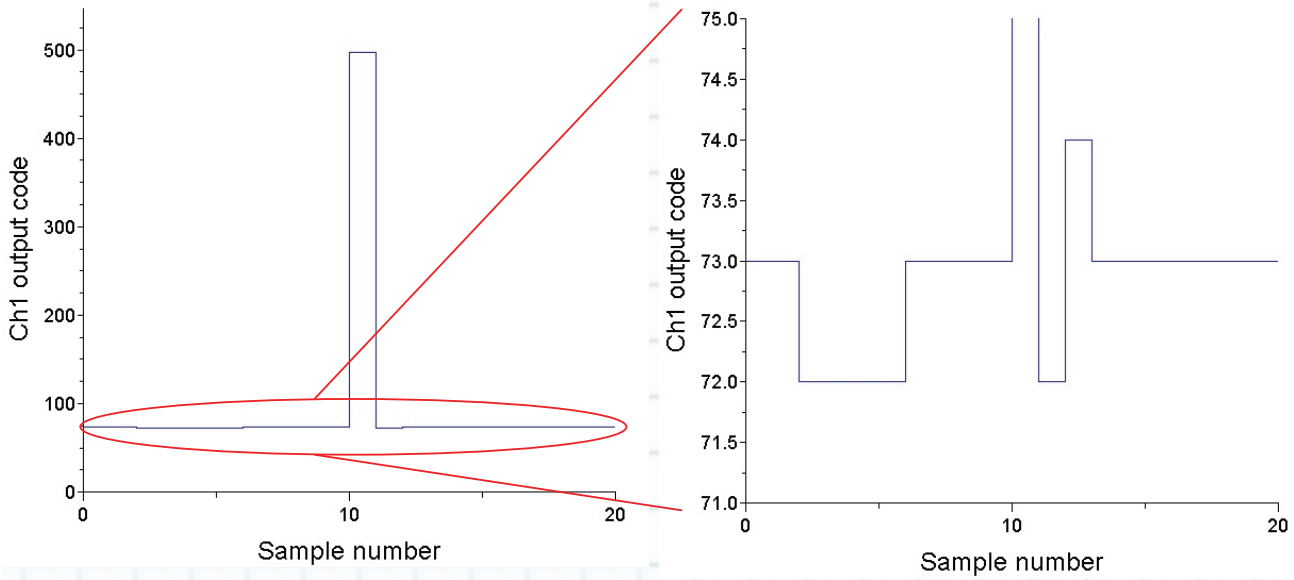


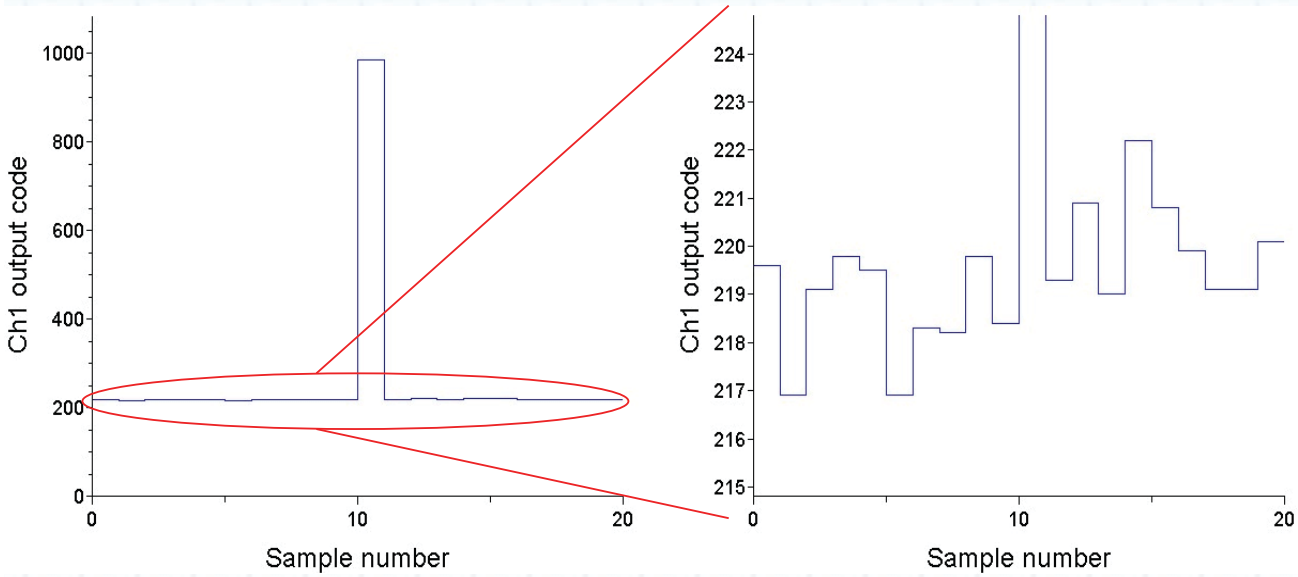
Bandwidth, SDT mode

- Input injected on 10th cycle only
- Digital output recorded, nominal speed



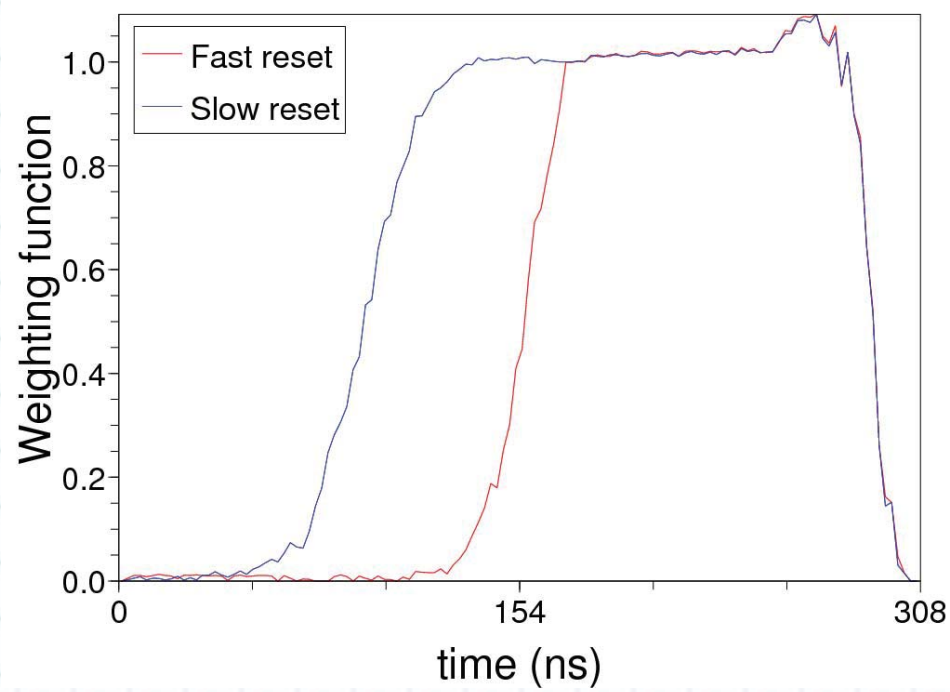
Bandwidth, DCal mode

- Input injected on 10th cycle only
- Digital output recorded, nominal speed



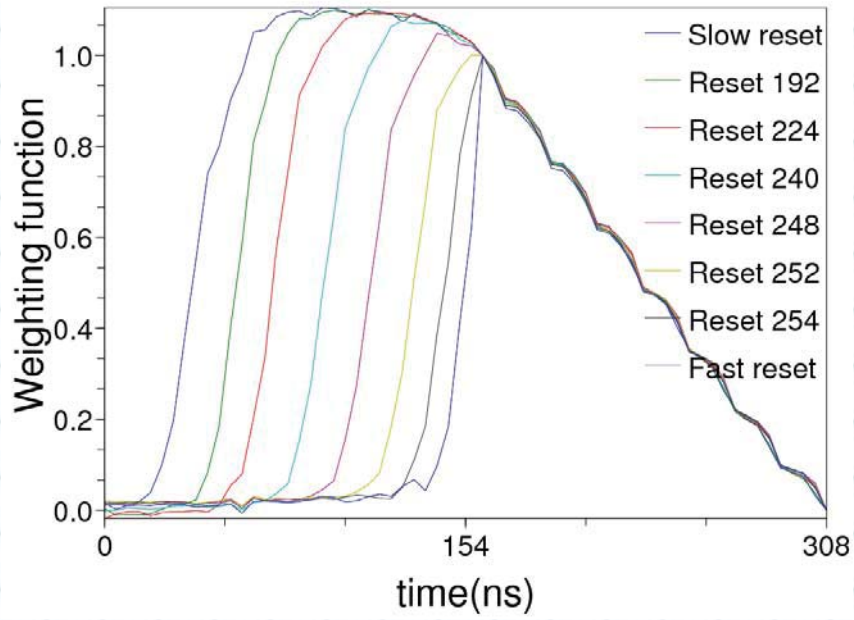
Weighting function, SDT mode

Time resolution: 4.8 ns



Weighting function, DCal mode

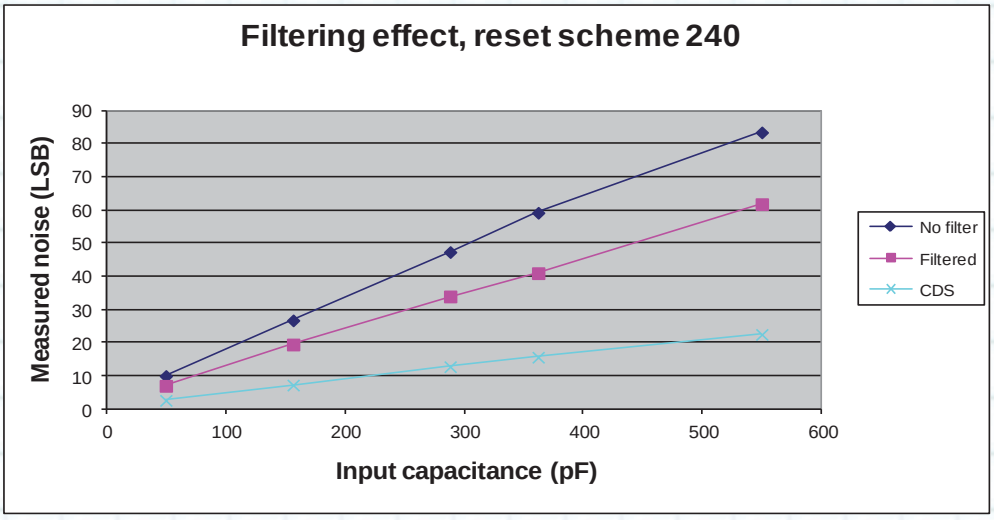
Time resolution: 4.8 ns



Noise filtering

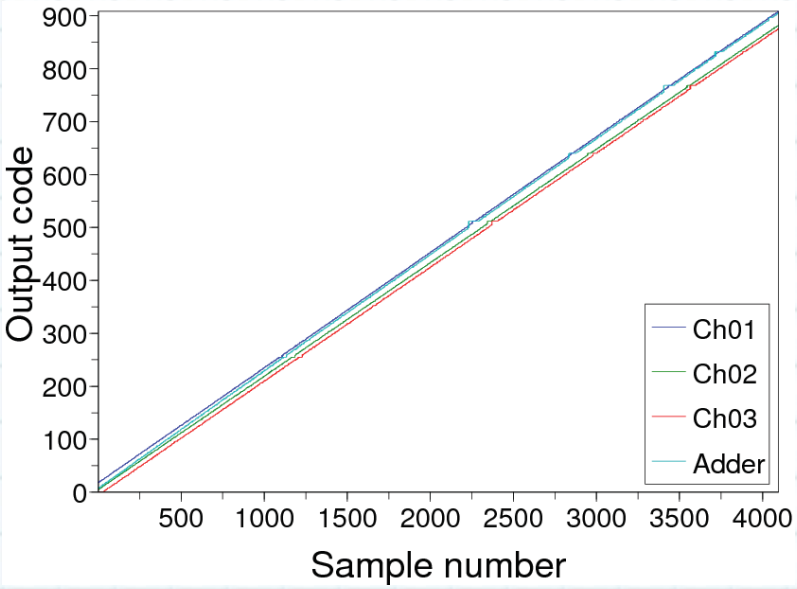
At 1.63 MHz clock (32x slower than nominal speed),

- Filter reduces series noise by 26% (same reset scheme)
- Filter + digital CDS reduces series noise by 73%
- Measurements deviate 0.52% from weighting functions calculations



Fast feedback adder test

- Adder proved full functionality at nominal speed of operation
- Gains from individual channels to Adder range from 0.329 to 0.345



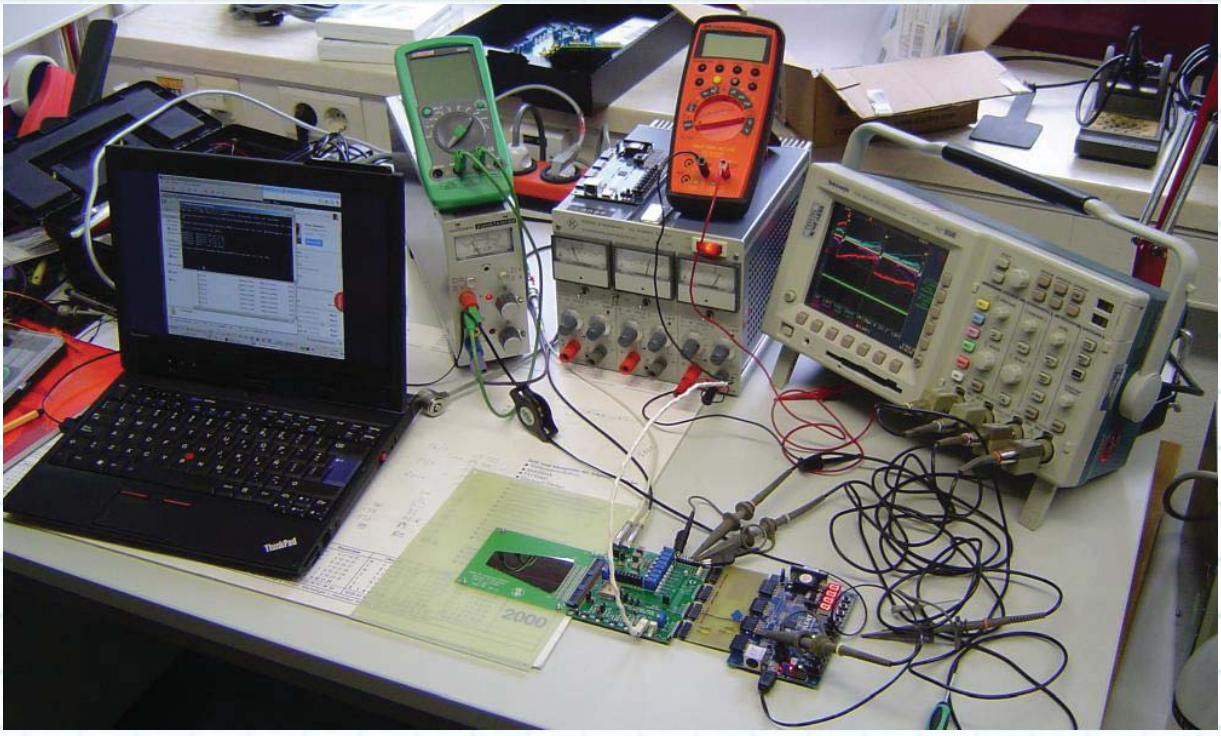
Test results - Summary

- The good
  - 100% occupancy, short recovery time
  - Very linear, and this can be improved even further
  - Fast feedback adder is fast in providing feedback
  - SC filter represents a competitive solution
  - Slow reset-release effectively reduces low frequency noise/reset noise (20% reduction in this chip)
- The bad
  - SC filters outperformed by CT filters
    - But are more flexible
  - Slow reset-release outperformed by CDS
    - But in some cases, slow reset-release can be a better/complementary option
- The ugly
  - Oscillating bias circuits – to be fixed
  - Noisy OTA – to be fixed

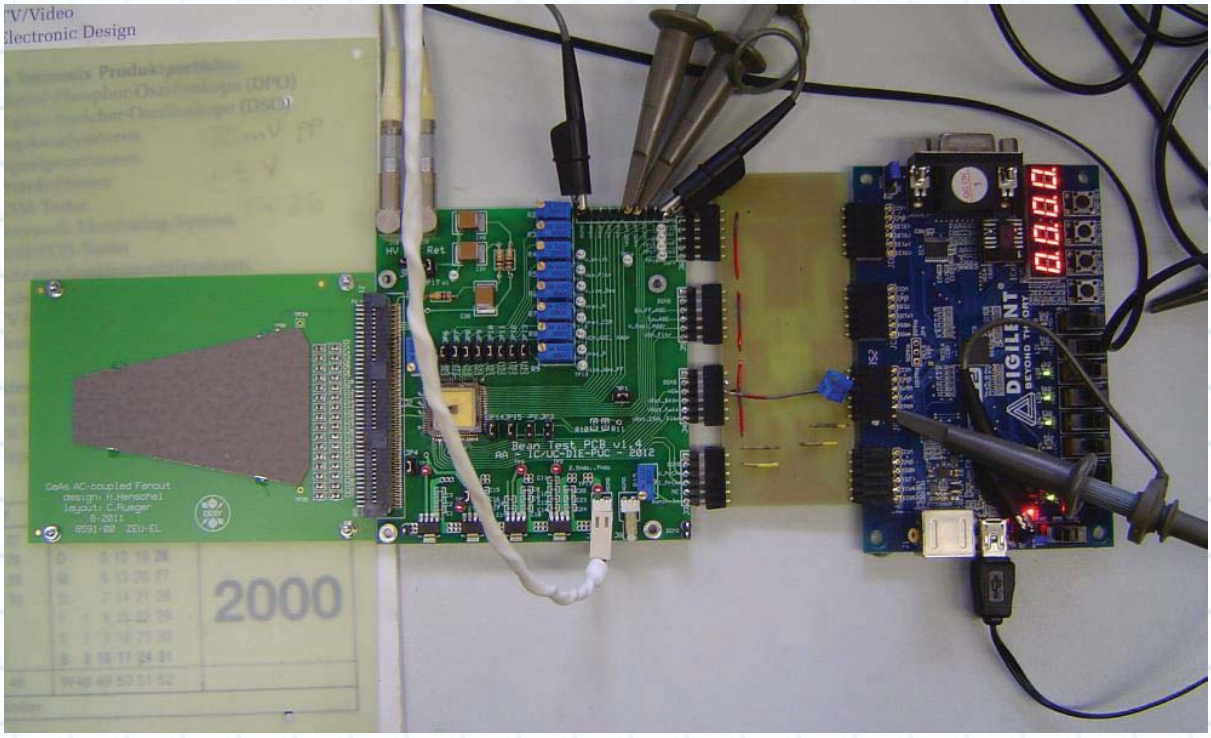
Testing @ DESY

- Initial tests at SLAC used a pulse generator on a discrete capacitor
- Currently testing the Bean with GaAs detectors
  - Different set of specs from what it was intended for, but…
  - So far, so good…

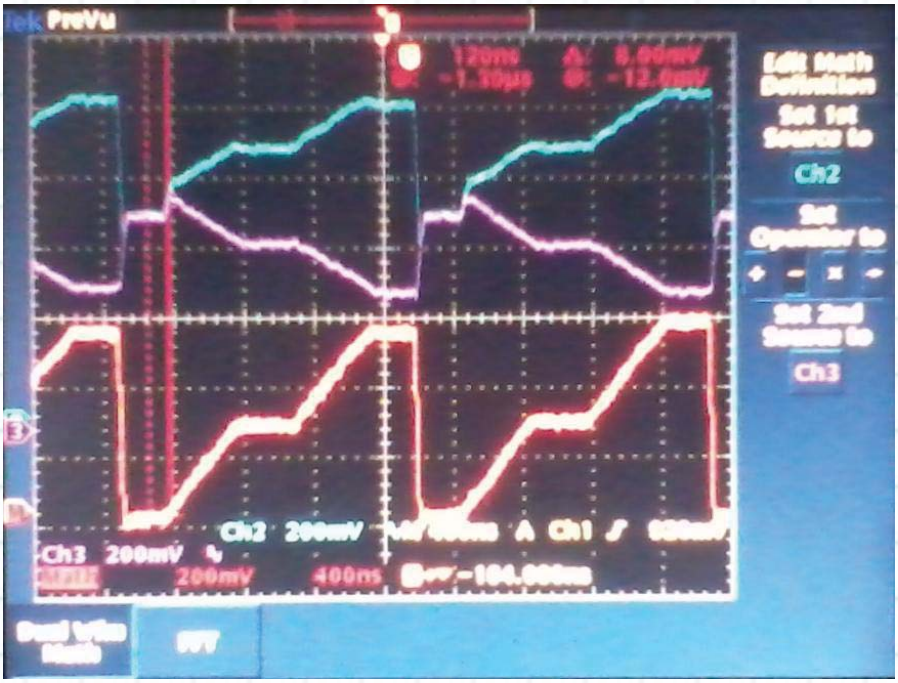
Current test setup



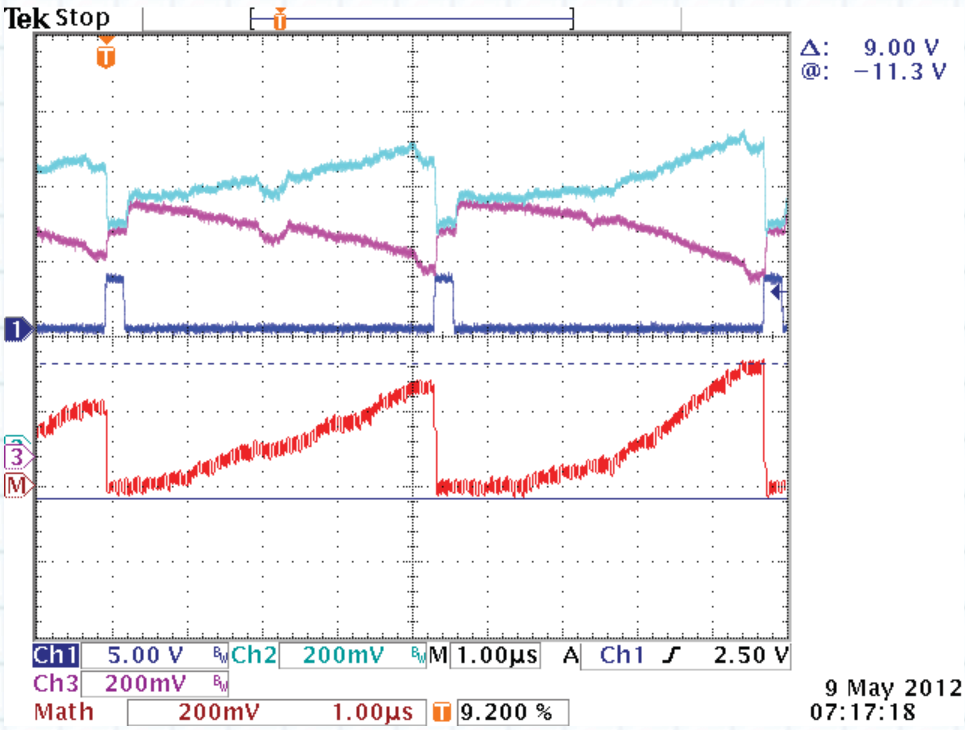
Close-up on the electronics



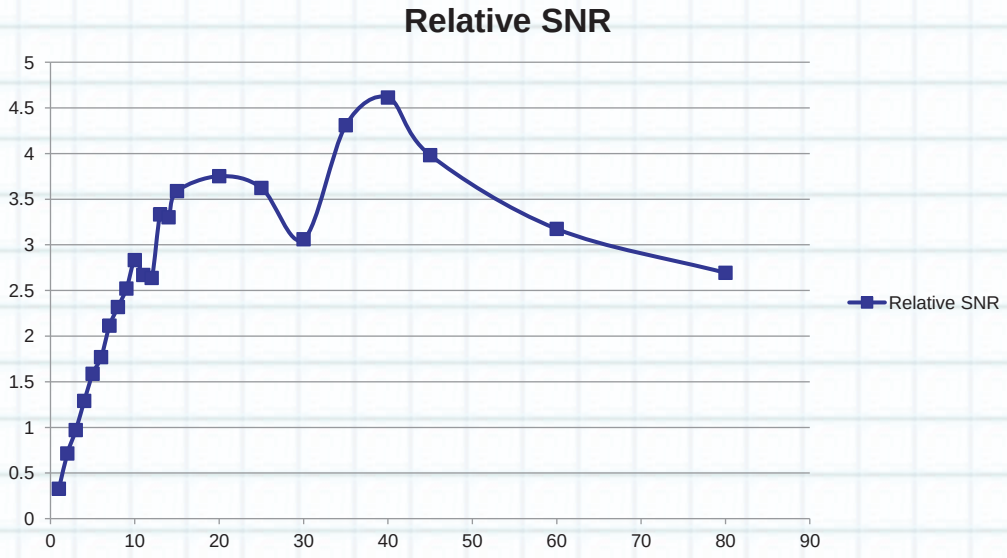
Some waveforms (no detector)



More waveforms (w/detector)



Optimal integration time



Current research

- Recent grant from Commission for Scientific and Technological Research (CONICYT) of Chile through FONDECYT program (2011 – 2014)
- 3 excellent students focused on analog IC design right now, more to come…
  - In Chile, this cannot be taken for granted at this time…
- Currently designing next version of the Bean chip
- Research topics:
  - ADC design
    - Power cycling, linearity compensation
  - Filter design
    - Arbitrary weighting function generation
    - Noise analysis for SC filters

Planned work

- 2012: Noise analysis on SC filters
- Aug. 2012: ADC tape out
- Early 2013: ADC tests
- 2013: Front-end design and tape out
  - Same technology node, different foundry
  - Including power cycling features
  - Arbitrary weighting function
  - Built-in CDS (analog domain)
- Early 2014: the Bean 2.0 first tests

Publications

- A. Abusleme, A. Dragone. G. Haller and B. A. Wooley. *BeamCal Instrumentation IC: Design, Implementation, and Test Results.* IEEE Transactions on Nuclear Science, in print.
- E. Álvarez and A. Abusleme. *Noise power normalisation: extension of gm/ID technique for noise analysis*. IET Electronics Letters, Vol. 48, No. 8, April 2012.
- A. Abusleme, A. Dragone, G. Haller and B. Murmann. *Mismatch of lateral field Metal-Oxide-Metal Capacitors in a 180-nm CMOS Process*. IET Electronics Letters, Vol. 48, No. 5, March 2012.
- A. Abusleme, A. Dragone. G. Haller and B. A. Wooley. *BeamCal Instrumentation IC: Design, Implementation and Test Results*. In Nuclear Science Symposium (NSS), Oct. 2011.

- More to come (under review and to be submitted), related topics…

Questions?

- Contact info:

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