Progress with the CPCCD and the ISIS

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The Linear Collider Flavour Identification (LCFI) collaboration is continuing the R&D towards a CCD-based vertex detector for the International Linear Collider (ILC). We are working on two detector technologies, the Column Parallel CCD (CPCCD) and the In-situ Storage Image Sensor (ISIS). The evaluation of our second generation CPCCD (CPC2) and its readout and driver chips is presently in an advanced stage. In stand-alone mode CPC2 achieved operation at 45 MHz, which is a major milestone. After the successful proof-of-principle first generation ISIS1 we are now planning to continue with new, more advanced device. In this paper we present the status and the tests results from our CPCCD and ISIS developments.

1 Introduction

ILC will require high performance vertex detector for accurate reconstruction of decay chains, pure and efficient b and c tagging and vertex charge measurements [1, 2]. The vertex detector has to improve significantly upon the most accurate one built so far, the VXD3 [3], with several times better impact parameter resolution, lower mass and sparse readout. Charge coupled devices (CCD) were used as sensors in VXD3 due to their high resolution, excellent gain uniformity and small layer thickness, which makes them one of the most likely candidates for the vertex detector at the ILC.

CCDs are well suited for linear collider environments [4] because of the much cleaner interactions and low backgrounds compared to those at hadron colliders. The small CCD pixels (20×20 μm^2 or below) allow excellent spatial resolution and two-track separation. This is helped by the low power dissipation, allowing the use of extremely low mass support mechanics. Large granularity, e.g. 2500 pixels/mm^2, permits integration of many events without loss of information due to overlaps. The CCD structure has 100% fill factor and all the active components are placed at the ends of the chip, which is very attractive for applications such as particle detection and imaging. Additionally, devices with an area of tens of square centimetres are readily available, which allows one to build detectors with optimal geometry.

2 Development of the CPCCD and its readout and drive systems

2.1 CPC2

Following the successful tests of our first CPCCD and its readout chip, the next generation devices CPC2 and CPR2 were designed and manufactured. An important new development in CPC2 is the busline-free design for clock distribution. In this architecture the clocks propagate on two separate metal layers covering the entire image area of the CCD. This

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drastically reduces the parasitic resistance and inductance associated with the conventional CCD buslines and enables efficient clocking at high speed.

Three sensors with common design and functionality, but different size were manufactured by e2V Technologies. The largest CPC2-70 has an image area of 92×15 mm^2 and total size of 105×17 mm^2, allowing for 2 bump-bonded readout chips. This device is almost the size needed for the outer layers of the vertex detector at the ILC. The middle size CPC2-40 (53×15 mm^2 image area) represents half of the inner layer of the vertex detector and is being used for tests at speeds up to the design goal of 50 MHz. The smallest chip CPC2-10 (13×15 mm^2) covers most of the test program because of the large number of available devices.

In the first tests the busline-free CPC2 was driven by miniature air core transformers, embedded in a multi-layer PCB and fed from power RF amplifier. We observed X-ray signals from a ^{55}Fe source (5.9 keV, producing 1620 electrons) at clock frequency up to 45 MHz. The performance was dominated by the numerous parasitics of the PCB transformers and the high levels of noise from the RF amplifier. Despite this, the result is very close to the desired clock speed and an important milestone for the LCFI collaboration.

2.2 CPR2

The second generation readout chip CPR2 builds on the experience gained with CPR1 and has already been manufactured and delivered. In addition to the banks of voltage and charge amplifiers, matched to the outputs of CPC2, CPR2 implements cluster finding logic on 2×2 pixel kernel and sparse readout circuitry. Numerous test features have been provided, such as direct analog inputs and outputs from selected amplifiers, scan register for independent tests of the sparsifying logic and direct monitoring of any ADC channel. The clock distribution network has been improved to reduce the differential nonlinearity of the ADCs.

The chip logic continuously calculates the cluster sum of 4 pixel signals from every 2 adjacent columns. Upon exceeding a global threshold, an area of 4×9 pixels around the cluster is flagged for readout and later multiplexed to the 5-bit wide chip output. Using the scan register, the sparsification logic was tested with simulated clusters and showed good operation. It was found that CPR2 exhibits variable dead time between clusters separated in time by less than 60 to 100 pixels. The reason for this is understood and will be corrected in the next, improved version CPR2A.

The design of CPR2A is in an advanced stage. The local memory buffer for the sparsification logic has been increased to hold 3 separate readout clusters instead of just one in the CPR2. The size of the cluster has been reduced to 4×6 pixels and the logic has been re-designed to efficiently store up to 3 consecutive clusters using the same timestamp, thus saving memory space. In addition, each cluster finder column will have individual 7-bit threshold, needed to correct for gain non-uniformities in the signal amplifiers. These measures will significantly improve the chip's capabilities to process groups of dense hit patterns and reduce dead time.

2.3 CPCCD driver chip

The gate capacitance of the busline-free CPC2-40 is 40 nF/cm^2/phase and current in excess of 20 Amps is required to drive it at 50 MHz. We designed a dedicated driver ASIC, the CPD1, made on 0.35 μm CMOS process. It uses optimised layout techniques for achieving minimum parasitic inductance in the clock and power paths. CPD1 is nominally supplied

with 3.3 V and the user can switch each of the 8 sections individually, as well as control the slew rate of the output clocks via digital register. CPD1 has a built-in capacitor, internally connected to one of the sections, which allows testing on an equivalent load of 32 nF with minimum parasitic impedance. The results at 50 MHz show excellent performance. We believe that similar performance could be achieved by bump bonding the CPD1 chip to a next generation CPCCD because of the very low interconnection impedance.

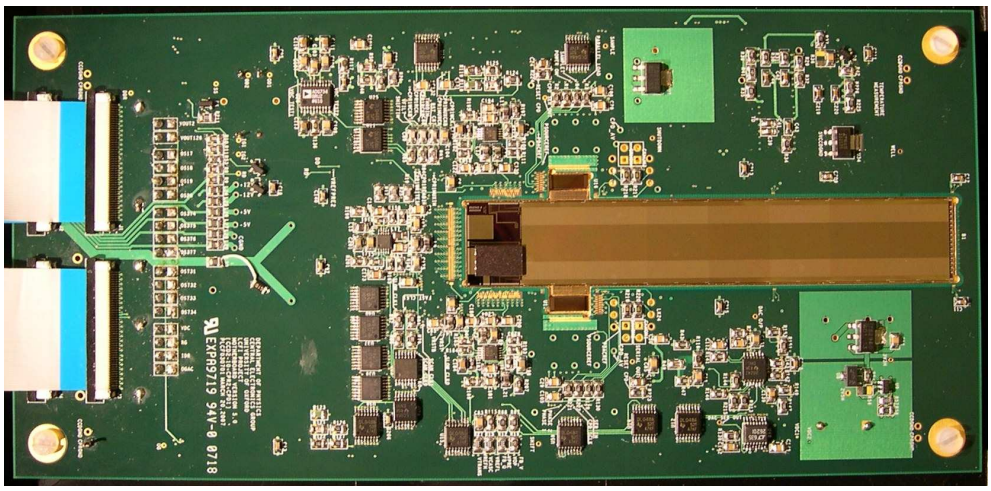

Figure 1: A prototype board with CPC2-70 (105 mm-long CPC2), bump-bonded to a CPR2 and driven by two CPD1 chips.

2.4 System tests

We developed a prototype board for testing all aspects of the three chips described above, shown on Fig. 1. Presently the driver chips are connected by wire bonds, which is not optimal for achieving the design readout rate due to their high parasitic inductance. However, the board has all the ingredients of a prototype ladder and is an important testbed towards building full-scale detector modules. Intensive tests of this configuration will be carried out in the following months.

3 Development of the ISIS

In parallel with the CPCCD development, LCFI is pursuing another CCD-based sensor, the In-situ Storage Image Sensor (ISIS) [5]. In every pixel of this device there is a CCD with 20 storage cells and 3-transistor readout circuitry, similar to that used in the Monolithic Active Pixel Sensors (MAPS). Charge generated by Minimum Ionising Particles (MIP) is transferred and stored in the CCD 20 times during the 1 ms-long bunch train at ILC. Readout is initiated in the 200 ms-long gap between the bunch trains at 1 MHz rate, using column parallel architecture. One of the main advantages of the ISIS is immunity to beam-related electromagnetic interference, because the signal is kept in the charge domain during the beam duration. In addition, the ISIS could be orders of magnitude more radiation resistant

than the CPCCD due to the reduced number of charge transfers. One could also achieve lower readout noise because of the relaxed clock frequency, allowing longer shaping times.

Together with e2V Technologies, LCFI has designed and manufactured the first ISIS device (ISIS1), based on a standard CCD process, and utilising deep diffused p+ well for charge shielding of the CCD register. The device is an array of 16×16 ISIS pixels, each containing a 3-phase CCD with 5 cells, reset transistor, source follower and a row select transistor. Due to process limitations the pixels are laid on 40 μm × 160 μm pitch and no on-chip logic for row selection and clocking is provided. The initial tests of the ISIS1 used pulsed light for charge generation and showed correct capture and transfer of signal into the CCD pixels corresponding to different time samples. Later the device was successfully tested with 5.9 keV X-rays as well, the results of which are shown in [6].

The development of a next-generation ISIS with 20×20 μm^2 pixel size is an ambitious goal which LCFI is actively pursuing. The combination of active transistors in every pixel, logic circuitry and CCDs in one monolithic device is challenging and will most likely require modifications to an existing CMOS process with feature size below 0.25 μm.

4 Conclusions

The work at LCFI towards a CCD-based vertex detector for ILC is advancing. Our second generation CPC2 is a large device and a major step towards detector-scale demonstrator. Stand-alone tests have shown successful operation at 45 MHz using the developed busline-free devices. The readout chip for CPC2 has also been successfully designed, manufactured and tested. A new, improved version of the readout chip is in an advanced design stage. The CPD1 driver ASIC has shown satisfactory performance driving large currents at frequencies up to 50 MHz.

The CCD-based ISIS concept has numerous advantages tailored for the ILC environment and is an extremely promising device for the future vertex detector. The first prototype has already been manufactured and the initial tests have been successful. The second generation ISIS will be made on a smaller pitch which will take it a step closer to satisfying the challenging detector requirements.

5 Acknowledgements

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