Study of SOI, 3D and Laser Annealing as Candidate Technologies for the ILC

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We have been studying SOI (Silicon On Insulator) and 3D technologies for integration of sensors and electronics as candidates for the ILC vertex detector. We have also been investigating laser annealing and its usage to form the ohmic contact at the backside of thinned sensor wafers. We will summarize these studies and present measurement results qualifying feasibility of these technologies at ILC.

1 Introduction

SOI consists of a thin silicon circuit layer over an insulator, usually SiO_2, placed on a "handle" wafer. The result is the suppression of bottom junction which leads to lower parasitic capacitance enabling faster switching and operation with lower power consumption. This, in turn, makes it possible to have denser layouts, operation at higher temperatures (250^oC) with lower SEU (Single Event Upset) rate.

The technology has application in fields such as high speed processors (AMD Athlon-64), graphic processors (Play Station 3), high-speed serial data communications, ultra low power solar cells, satellite systems, spacecraft electronics and high energy physics (HEP). The handle wafer in SOI can be high resistivity silicon, making integration of detector and electronics possible.

The Fermilab group has initiatives in the following areas:

- Thinned, edgeless sensors
- Chip fabricated in OKI 0.15 μm SOI process, includes sensor and one layer of electronics for electron microscope
- Chip being designed in American Semiconductor 0.18 μm SOI process with pixel sensor layer and one or more electronics layers for ILC vertex detector
- 3D chip (VIP1) being fabricated in MIT LL 0.18 μm SOI multi-project run, a 3 tier demonstrator chip for ILC vertex detector
- Bonding Technologies being explored, such as Cu-Sn bonding of FPIX chips/sensors and DBI bonding of 3D chips to MIT sensors
- Laser annealing
- Simulations

2 SOI Concept for HEP

The SOI chip is formed by a high resistivity silicon handle wafer, thinned to 50-100 microns (fully depletable with large signal) separated from the transistor layer by a layer of Buried Oxide (BOX), as shown in Figure 1. The edges are activated and the back of the substrate has an Ohmic contact. The backside is implanted and laser annealed after thinning. SOI provides the possibility of monolithic fabrication of detectors and electronics, with low mode capacitance, full depletion and no parasitic charge collection as in CMOS MAPs.

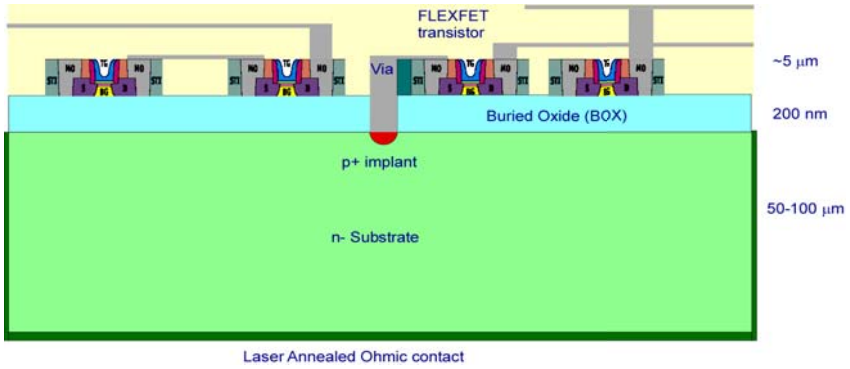

Figure 1: Schematic view of a SOI detector.

2.1 OKI 0.15 μm SOI process Mambo X-Ray Chip

Fermilab has submitted a design to a KEK sponsored multi project run at OKI which incorporates diode formation by implantation through a via formed in the BOX. The chip incorporates a 64 x 64 26 micron pitch, 12 bit counter array for a high dynamic range x-ray or electron microscope imaging. Maximum 13 μm implant pitch is determined by the "back gate" effect where the topside transistors thresholds are shifted by handle potential. It is 350 micron thick. We just received this chip and will test it at a laser test stand.

2.2 American Semiconductor 0.18 μm SOI process Flexfet Chip

Fermilab designed for American Semiconductor Company a demonstration SOI pixel cell with voltage ramp for time marker, sampling for crossing time, analog pulse height and counter for timestamp. All these features are simulated beforehand. Transistors in this chip have two gates. In addition to the conventional top gate, a bottom gate shields the transistor channel from charge buildup in the BOX caused by radiation, as well as from the voltage on the substrate and removes the "Back Gate Voltage" problem. Optimization is on-going on this chip and it is to be tested. Also, possibility of a pinning layer to shield the analog pixel from digital activity is considered.

2.3 VIP1 Chip

The goal of this chip, shown in Figure 2, which is being fabricated in MIT LL 0.18 μm SOI multi-project run, is to demonstrate the ability to implement a complex pixel design with all required ILC properties in a 20 micron square pixel. It is a three dimensional (vertical) integration of electronics and sensors, reducing R, L, C for higher speed, reducing chip I/O pads and providing increased functionality. Also, interconnects by through wafer via formation and metallization reduce the power and crosstalk.

Previous technologies limited to very simple circuitry or large pixels. This chip has three levels (also called tiers) of transistors, 11 levels of metal in a total vertical height of only 22 μm. Its key features are analog pulse height, sparse readout, and high resolution time stamps. Time stamping and sparse readout occur in the pixel. Hit address is found on array perimeter. It will be a 64 x 64 pixel demonstrator version of eventual 1K x 1K array. Edgeless sensor will be bonded to the chip later.

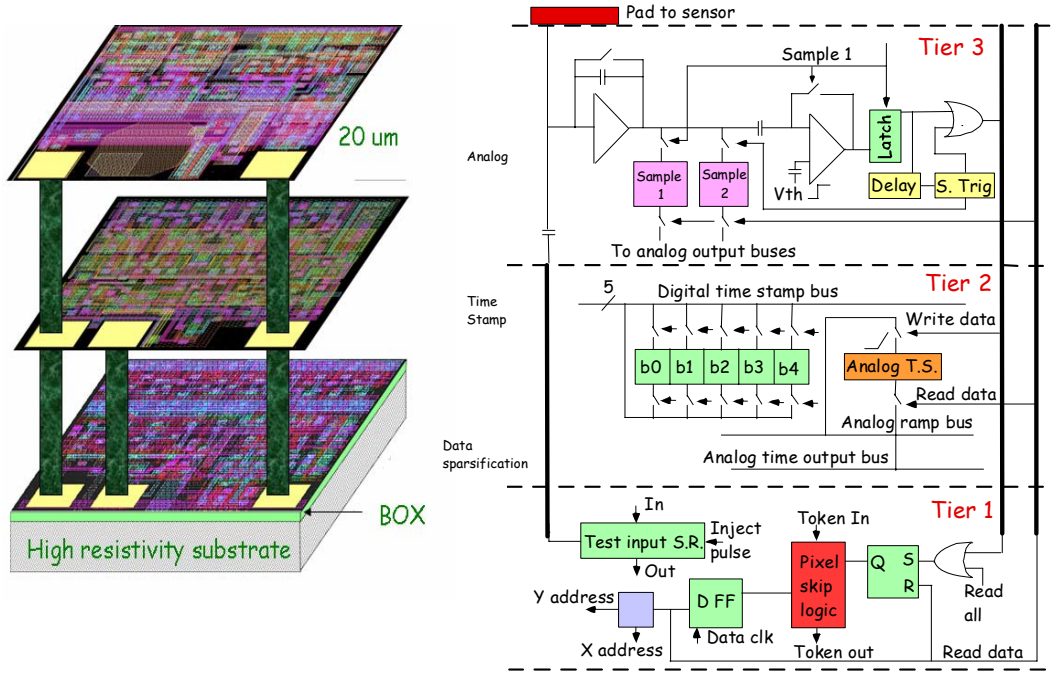

Figure 2: VIP1 Chip

2.4 Laser Annealing

After thinning a substrate, a backside contact must be formed. This is usually done by implantation and high temperature furnace annealing which will destroy the front side CMOS SOI circuitry. An alternative is the laser annealing of the backside implantation, which limits the front side temperature. Use of a raster scanned eximer laser melts the silicon locally. This activates the implant and repairs the implantation damage by re-crystallizing the silicon. Diffusion time of phosphorus, the ohmic material, in molten silicon is much less than cooling time therefore we expect uniform distribution in melt region. This was demonstrated by SIMS (Secondary Ion Mass Spectroscopy) measurements which provided implant depth profiles by analysis of ions ejected from the surface upon ion bombardment.

3 Acknowledgements

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Slides can be viewed at:

http://ilcagenda.linearcollider.org/contributionDisplay.py?contribId=309&sessionId=74&confId=1296