Prototype DAQ for Calorimetry at Future ILC Experiments

David Bailey[1] for CALICE-UK♦

1 – School of Physics and Astronomy, University of Manchester,
Oxford Road, Manchester M13 9PL

CALICE-UK are developing a prototype data-acquisition (DAQ) system for calorimeters at future ILC experiments. This DAQ system will be implemented using FPGAs and built using commodity components and networking hardware. The EUDET ECAL technical prototype will be used to demonstrate the feasibility of this approach. The design philosophy is presented, along with a possible implementation using PCI-express cards mounted in PCs, which act as data receivers and network interfaces.

Introduction

One of the most challenging aspects of calorimetry at the ILC is to successfully implement particle flow. This technique is the leading candidate to achieve the required excellent jet energy resolution vital to exploit the physics potential of the machine. The key to successful particle flow is a highly granular calorimeter, allowing the clean separation of showers from individual particles – in essence a tracking calorimeter. This approach leads to the requirement to handle very large quantities of data from the many readout channels.

The beam structure of the ILC, with a bunch train of 1 ms duration followed by a quiet gap of 200 ms, requires the detector readout electronics to digitise and time-stamp and buffer data from each bunch crossing during the bunch train and then read out the entire data sample during the inter-train gap with no triggering. All event classification and selection will be performed quasi-online by processor farms, so the main task of the DAQ is to send the data to mass-storage with no deadtime. It is also vital that no data be lost through buffer overflows or congestion in the network. Figure 1 shows the philosophy of the DAQ design.

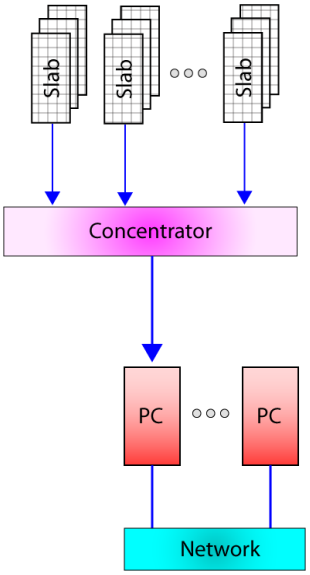

Figure 1: The DAQ uses a classic funnel design, concentrating the data in stages before sending it to storage.

Due to the very high number of readout channels and the necessity to minimise costs it is highly desirable to use commodity components wherever possible instead of developing bespoke solutions. This naturally leads to using powerful FPGAs and standard networking protocols as the building blocks of the DAQ system. Prototypes have been built using commercial FPGA development boards to receive data over Ethernet and store it to disk over PCI-express. Strategies for sending the data over a standard Ethernet-based network have also been investigated.

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The Front End

The detector signals are buffered and digitised by the Very Front End (VFE) ASICs. The interface to the VFE and DAQ system is provided by a sub-detector specific interface (DIF) board. This has been prototyped using a Xilinx Spartan FPGA development board. The VFE ASICs along the so called ECAL "slab" are emulated in FPGAs, allowing the development of the necessary control signals in the DIF. The DAQ interface is currently USB or Ethernet for simplicity of testing. Figure 2 shows the prototype system under test in Cambridge. It is anticipated that the production DIF will have a high-speed, bi-directional serial link to the DAQ and a connection to a neighbouring DIF for redundancy in case of failure of the primary DAQ link. The link to the DAQ must be shielded and the current implementation is envisages using HDMI cables to carry the serial data and a clock as they are compact, readily available and can be made halogen-free. It may also be possible to add a prompt signal, carried on spare conductors in the HDMI cable, to inject test triggers or provide an input for a cosmic trigger.

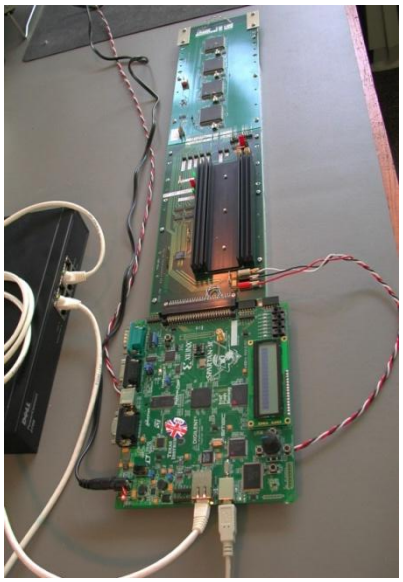

Figure 2: Prototype DIF connected to simulated EUDET ECAL VFE electronics.

It is envisaged that all the serial links will be encoded using 8B10B over LVDS.

DAQ System

A schematic of the on-detector DAQ system is shown in Figure 3. The first-level data concentrator (LDA in the figure) provides synchronous clock and control information to a number of DIFs. It also aggregates the data from the same DIFs. The redundant DIF-DIF connection is also shown. It provides a surrogate serial link for readout and a clock.

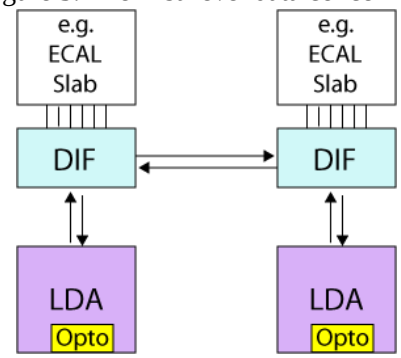

Figure 3: Schematic of the DAQ links between the front end electronics and first level concentrator (LDA).

The LDAs buffer and frame the data for transmission over long, optical links to the off-detector receiver infrastructure. The downstream (off detector) links need not be synchronous with the accelerator clock as meta-data will be added to the data stream so that it is completely self-describing. Depending on where the external clocks are connected to the DAQ system, it may be necessary for the upstream (i.e. to the detector) to be synchronous, fixed latency serial links. Regardless of this requirement on the off-detector links, all the LDA-DIF serial links must be synchronous and of fixed latency to ensure the

concurrent arrival of control signals at the VFE electronics. The complete DAQ system is shown schematically in Figure 4. Since all the sub-detector-specific control signals are generated by the DIF electronics, the entire DAQ chain from the DIF links to the off-detector infrastructure can be common between all components (subject to readout rate requirements) allowing commoditisation.

The off detector receiver (ODR) has been prototyped on a Xilinx Virtex4 development board supplied by PLDApplications [1]. A complete gigabit Ethernet layer has been implemented in the FPGA, capable of driving both optical and copper physical layers through the on-board SFP cages. This Ethernet capability has been used to investigate the data transfer rates over PCI-express from the card to disk and also to evaluate efficient network protocols to transfer data direct from the cards into packet-based networks [2]. At present the ODR is implemented using an FPGA on an PCI-express card, however if the ILC machine control infrastructure chooses to standardise on a crate-based system, such as ATCA, it would be possible to move the ODR systems to that infrastructure with minimal modification due to the use of standard network and interconnection protocols for data transmission.

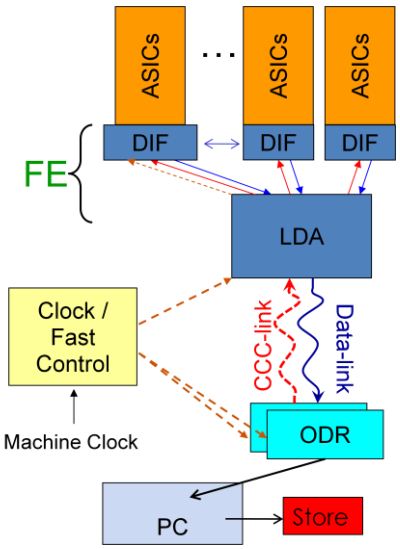

Figure 4: Schematic of the entire DAQ showing front-end, clock and control and off-detector components. Dotted lines indicate potential synchronous, fixed latency links.

The performance of the prototype ODR has been investigated using the Ethernet interface to provide an input data stream which is then subsequently written to the disk of the host PC. An example of the data-transfer rates to disk is shown in Figure 5.

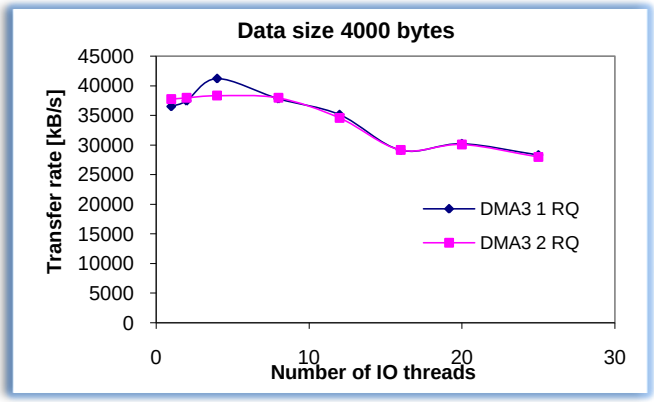

Figure 5: Example performance of the ODR data transfer rate to disk.

Summary

CALICE-UK are prototyping the major components of a high-rate, scalable DAQ infrastructure that is based on readily available commodity commercial components. It will be used to read out the EUDET calorimeter technical prototypes.

References

[1] http://www.plda.com. [2] See the proceedings of IEEE NPSS Real Time Conference 2007 for details.