BeamCal FE Electronics Status

FCAL Workshop

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SLAC NATIONAL ACCELERATOR LABORATORY

Outline

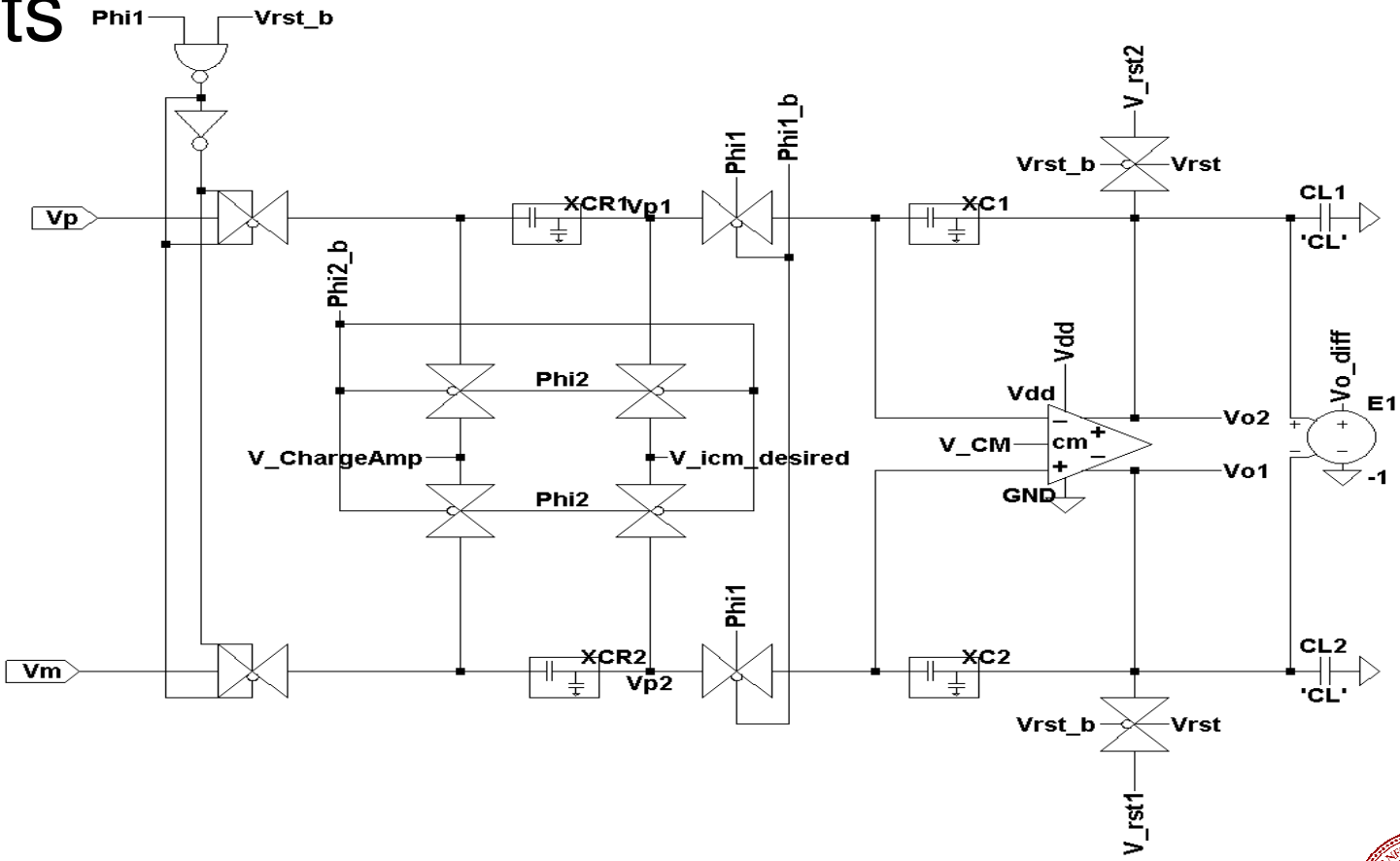
- Introduction
- ADC prototype circuit
- Front-end design status
- Tentative schedule
- Acknowledgements
- People

Introduction

(mainly stuff from previous meeting)

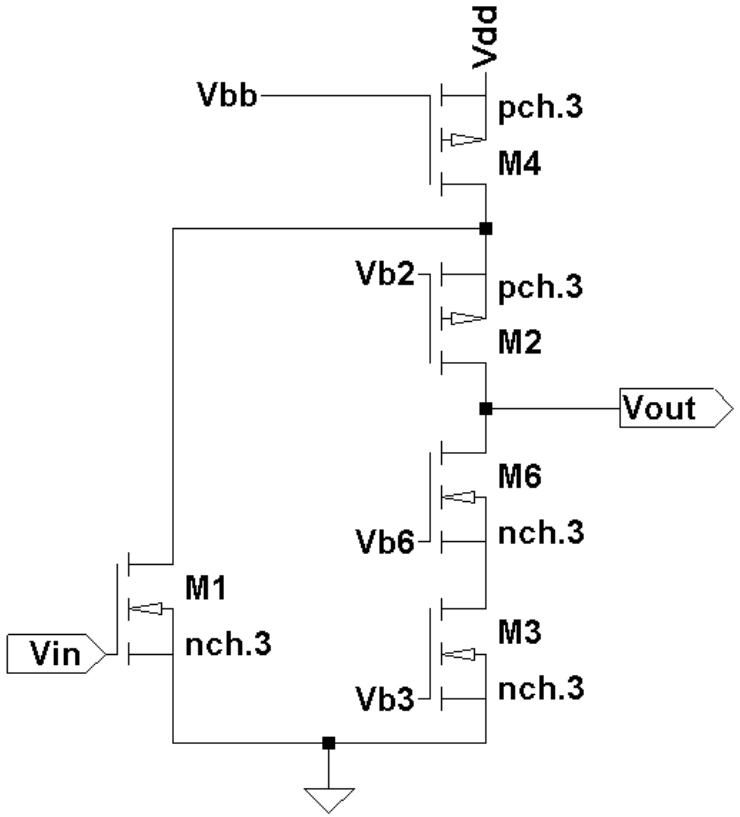
… from last meeting

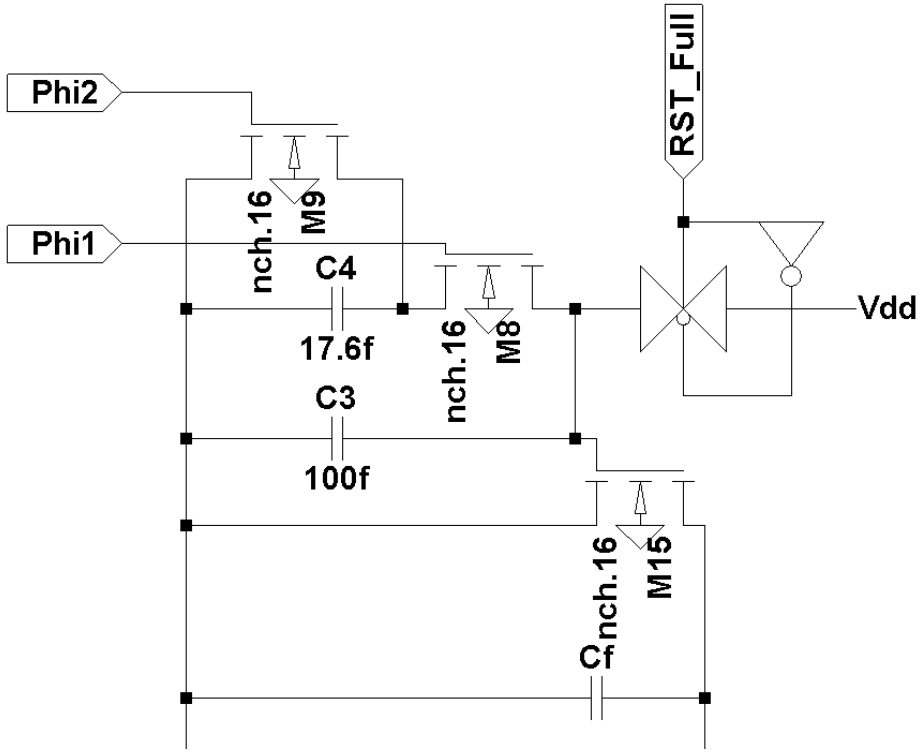
- FE implementation via switched-capacitor circuits



… more from last meeting

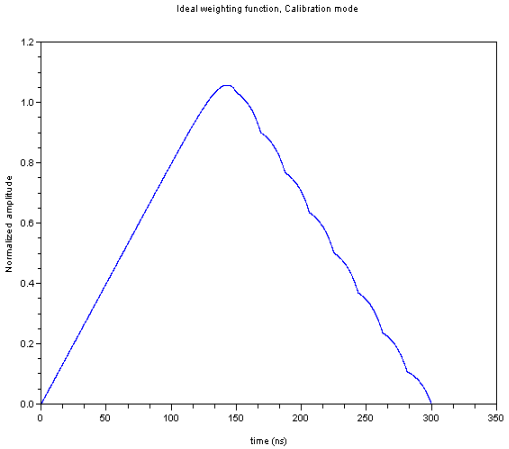
- Reset scheme via switched-capacitor circuits



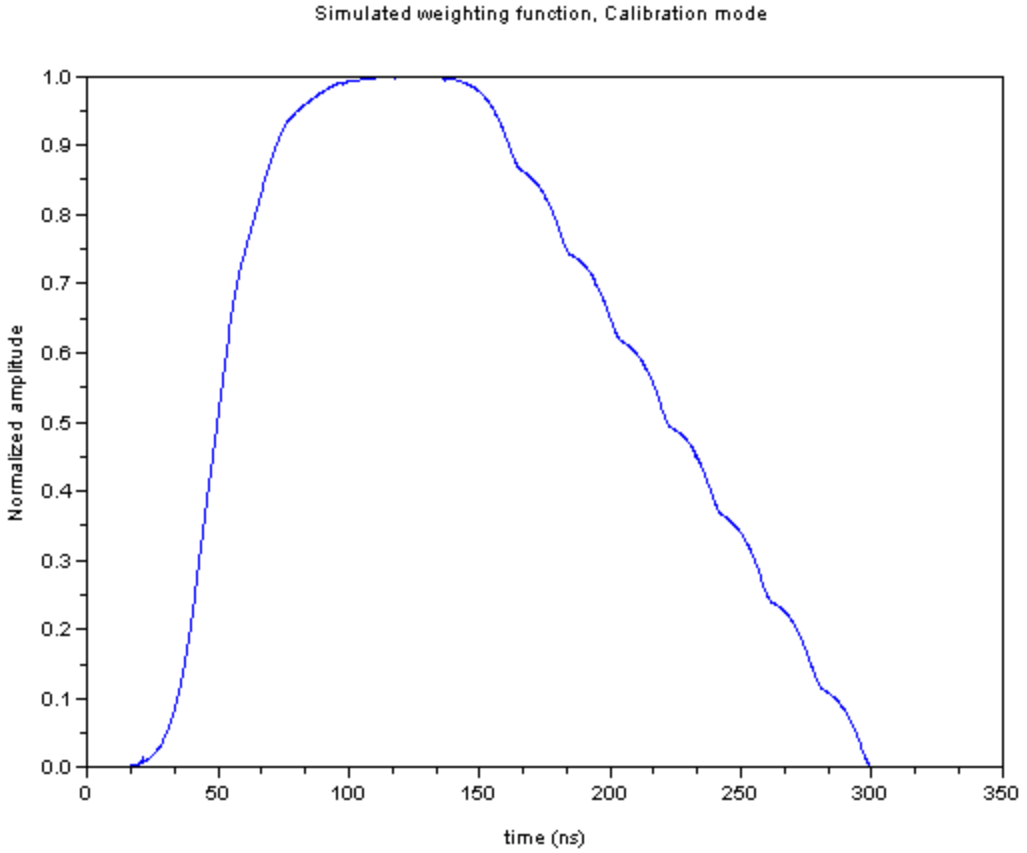


… still from last meeting

- Weighting functions precisely defined



ideal



… so what's new since last meeting?

- FE design was frozen
- ADC specifications were defined
- A prototype ADC was designed and fabricated, and currently being tested
- The FE design is in layout stage

ADC Prototype Circuit

ADC Prototype Circuit

- Required specifications
- System-level design
- Circuit-level design
- Layout
- Tests

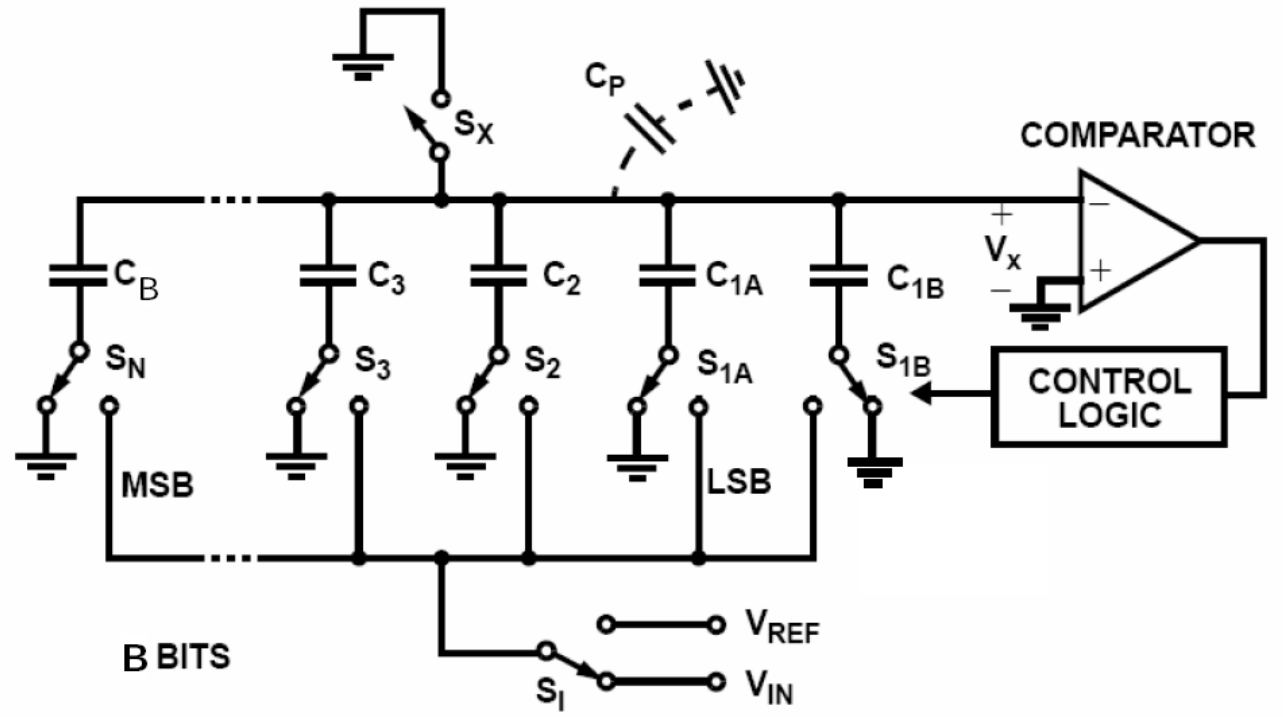
ADC specs

Specs given by channel high level design and FE circuit details

- Conversion rate: 3.25MHz
- Stated resolution: 10 bits
- Input capacitance: around 2pF
- Area, power: minimize (remember, one ADC per channel, 32 channels per chip)

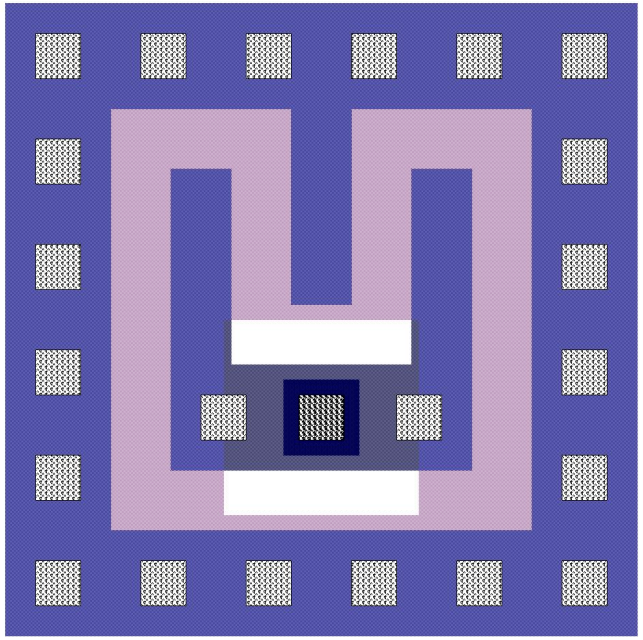
ADC System-level design

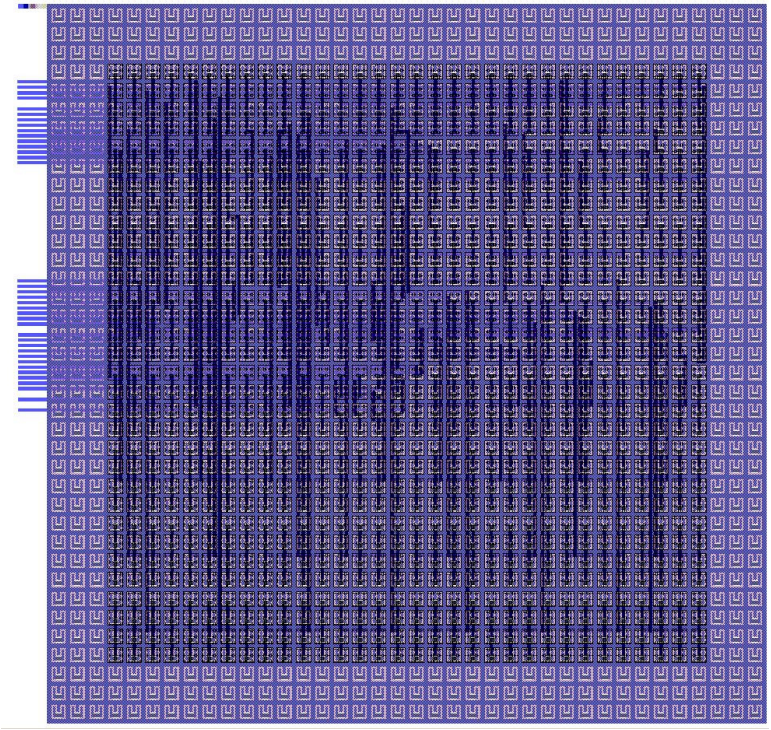
- Successive approximation ADC is chosen
- Switched-capacitor charge redistribution implementation (widely used, McCreary, JSSC 12/1975)



ADC System-level design

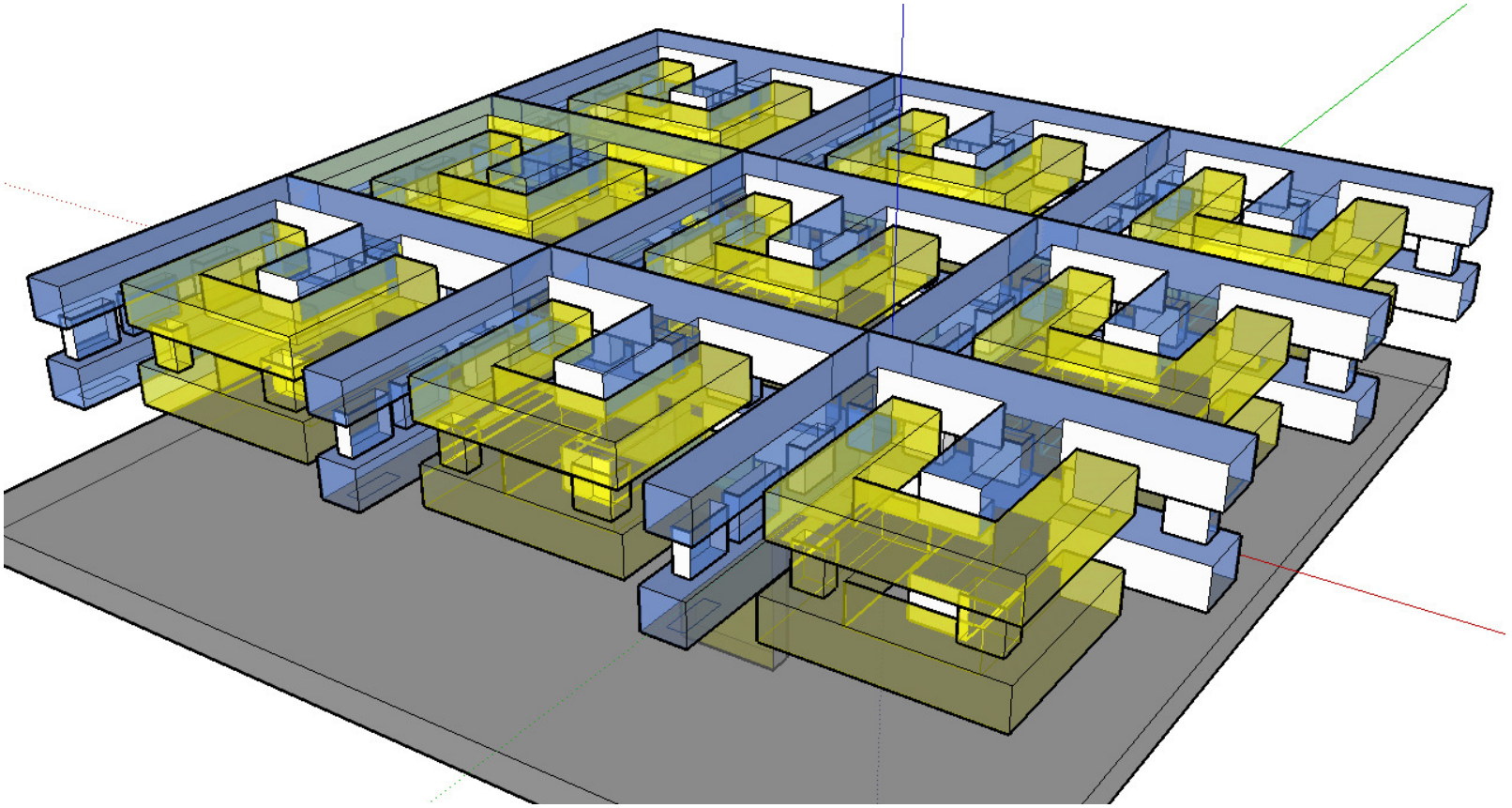
- Challenge: 10-bit resolution and 2-pF input capacitance
  - Implies a ~2-fF unit capacitor. Is it possible? Matching? We'll see…
  - Using metal-oxide-metal (MOM) custom capacitors, and SPACE3D software from Delft U. for analysis.





ADC System-level design

Capacitor array 3D view (not to scale)

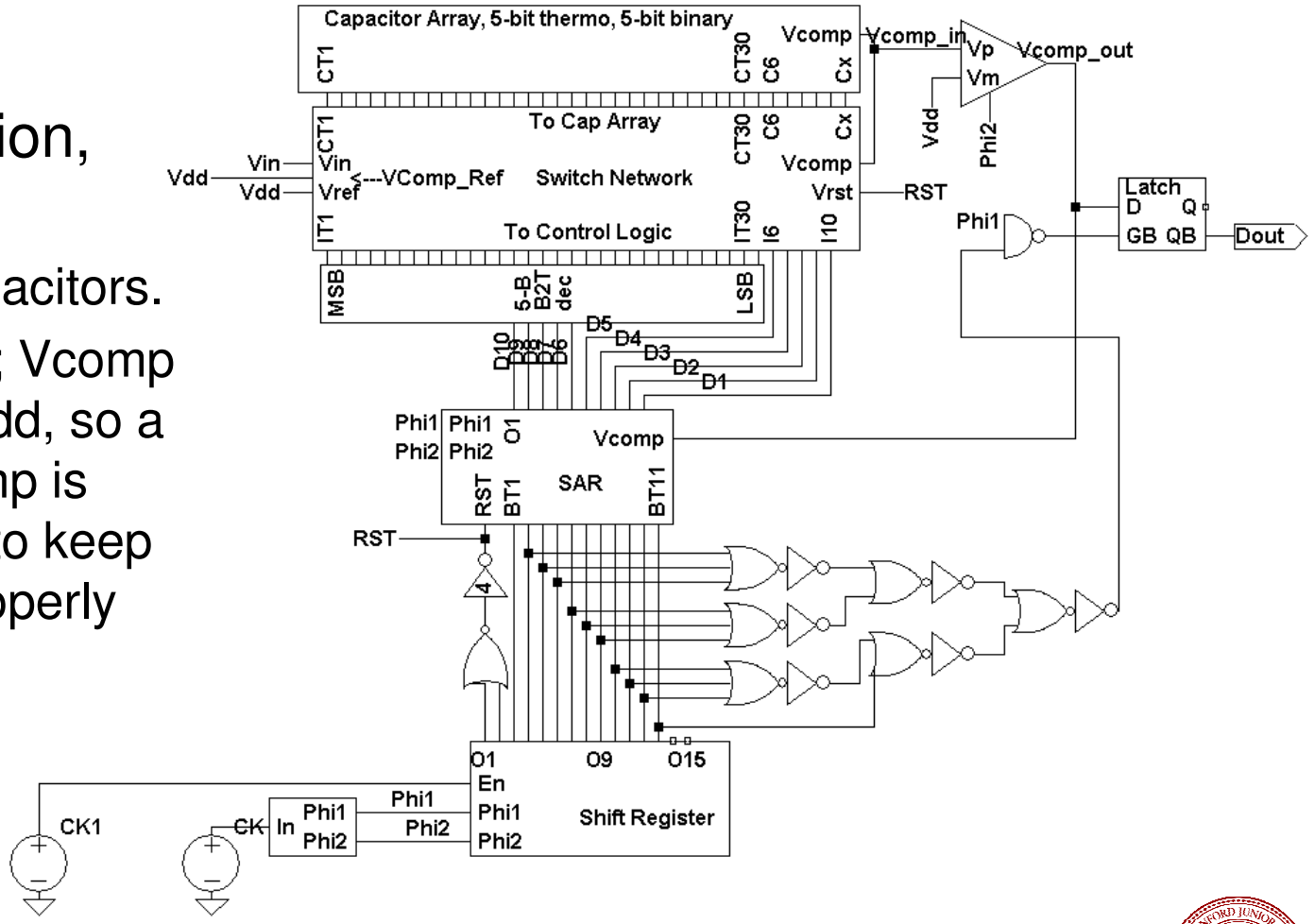


ADC System-level design

- How about cap. matching?
  - Not much data available…
  - To reduce matching requirements, 5 out of the 10 bits are thermometer-coded. This reduces differential nonlinearity.
  - Montecarlo simulations showed that 2% matching among unit caps is good enough (no missing codes). Maybe it is possible…

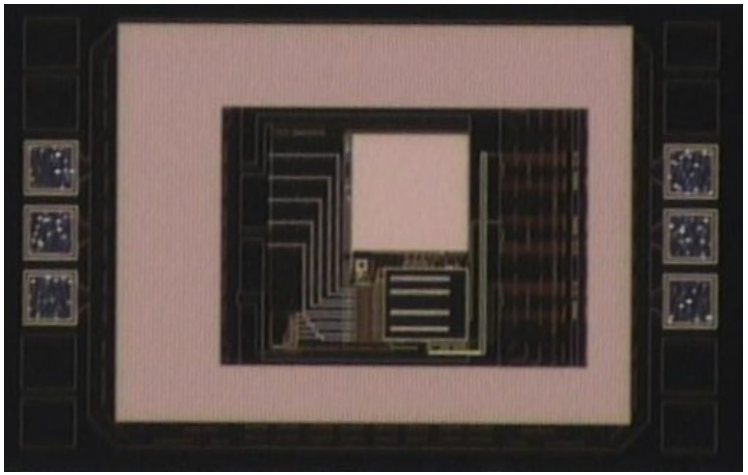
ADC circuit-level design

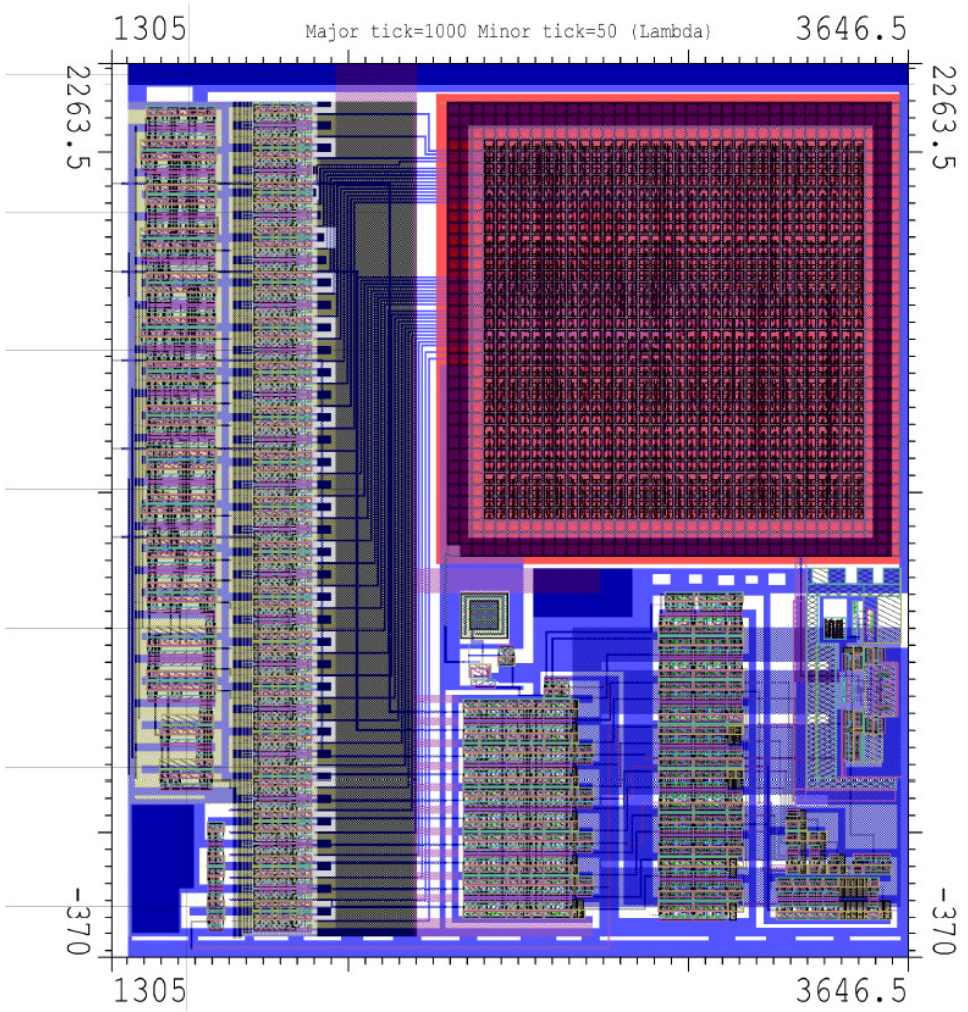
- … a pretty standard implementation, except for:
  - the tiny capacitors.
  - Vref is Vdd; Vcomp can be > Vdd, so a charge pump is necessary to keep all wells properly biased.



ADC layout

- Circuit & pad frame is 1mmx0.5mm, fabricated in TSMC025





ADC tests

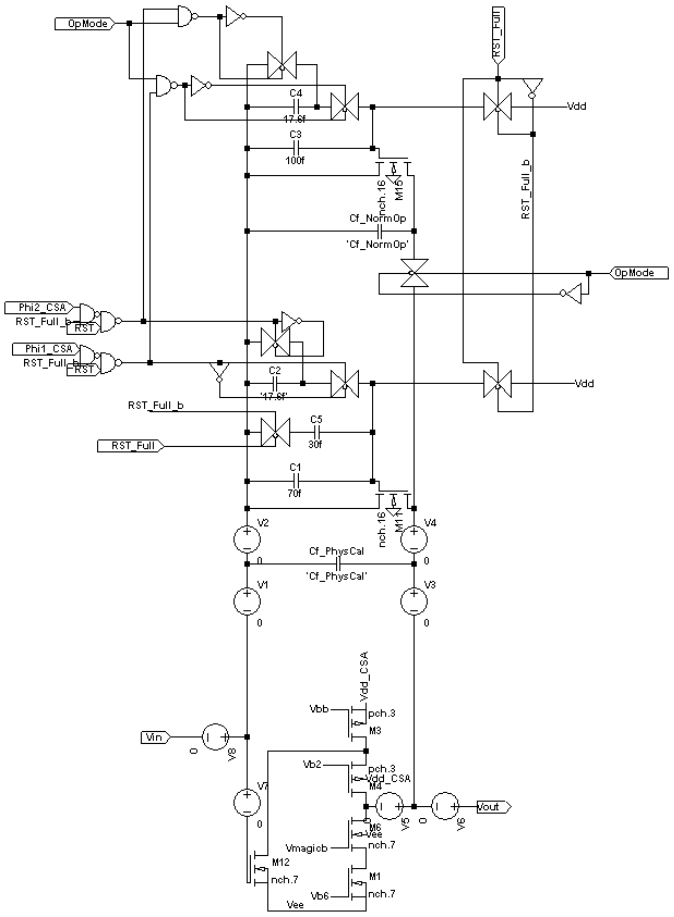
- Preliminary test results show that:
  - the ADC behaves like an ADC, and that
  - the input capacitance is very close (1%) to the design target value.
- Linearity measurements (DNL and INL) will allow us to estimate capacitance matching and the exact capacitance value
- We are currently working on this…

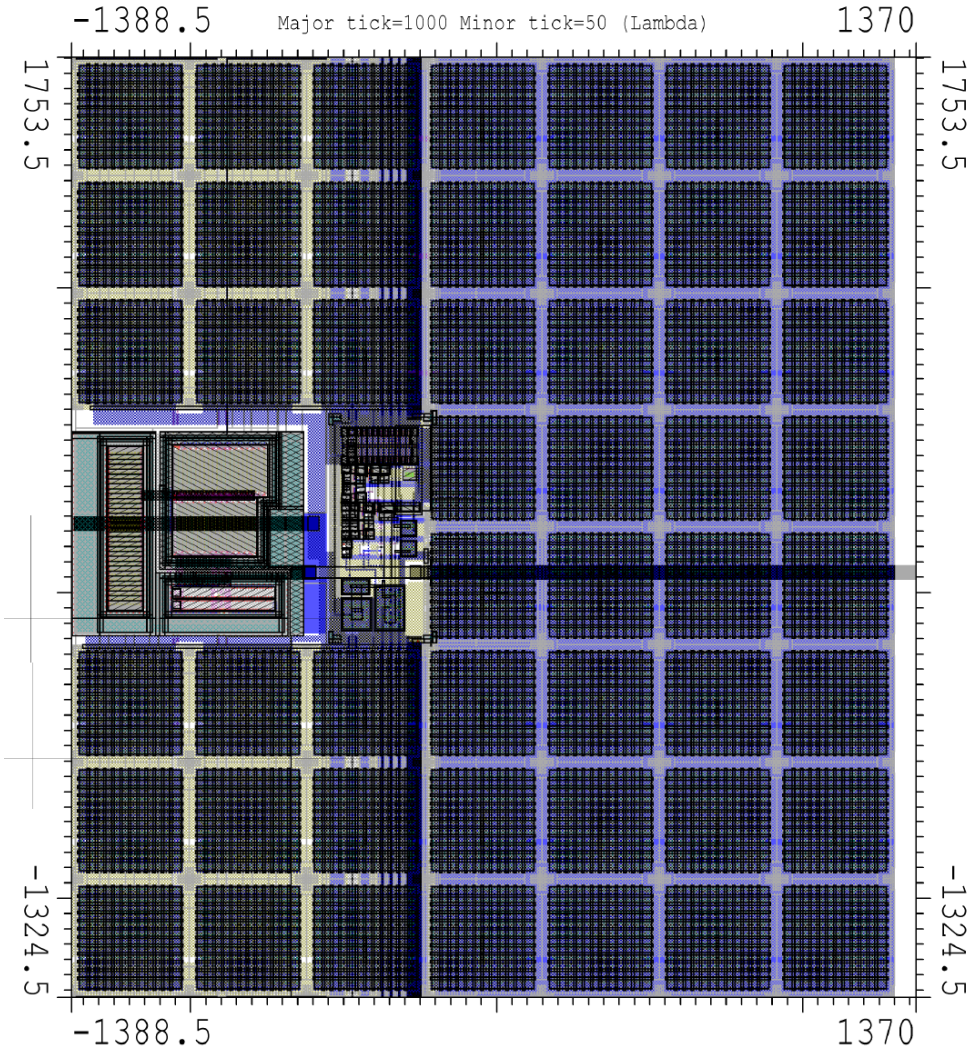
Front-End Design Status

Front-End Design Status

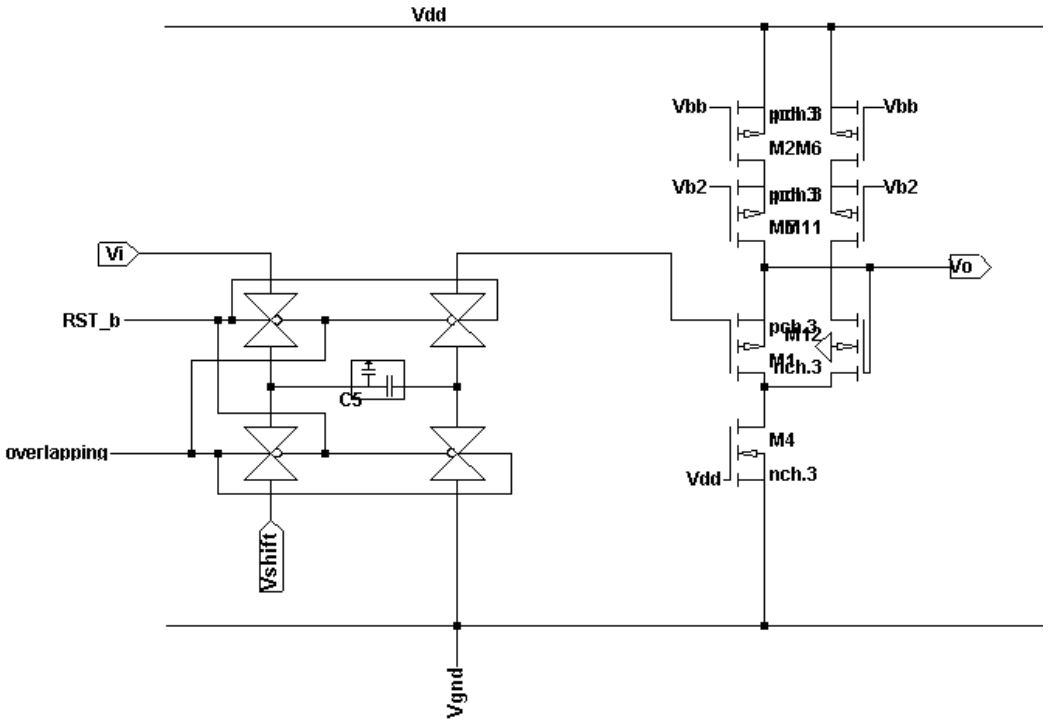
- The FE principle of operation (switched-capacitor filter and reset) has been extensively tested in simulations.
- It allows a low noise, dual gain measurement, in a 100%-occupancy system.
- The actual ASIC will allow us to prove the principle of operation…

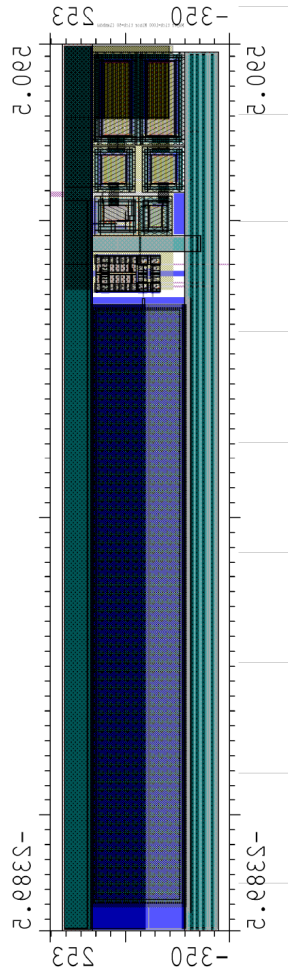
Preliminary layout: CSA



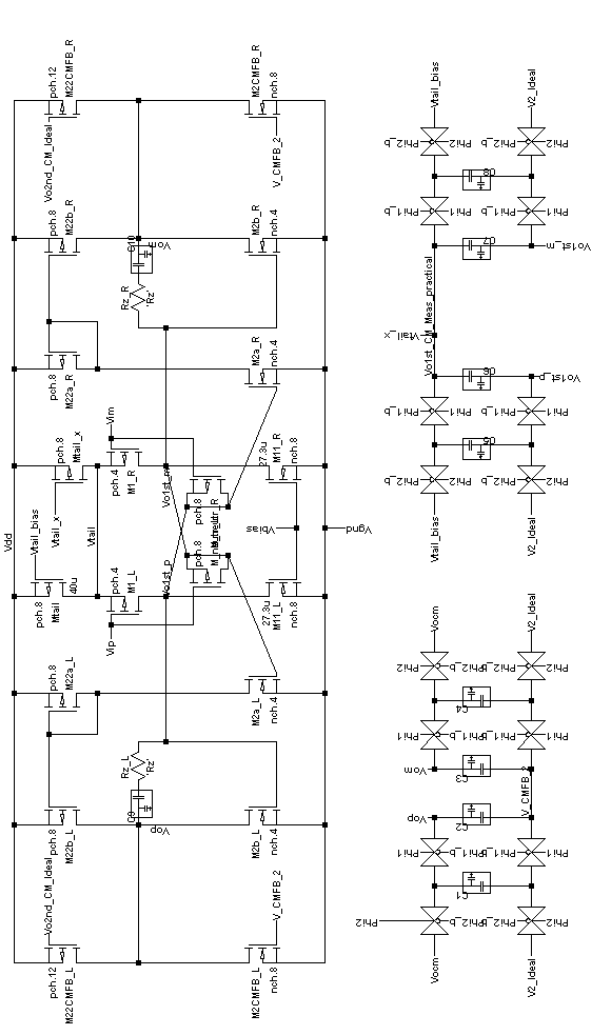


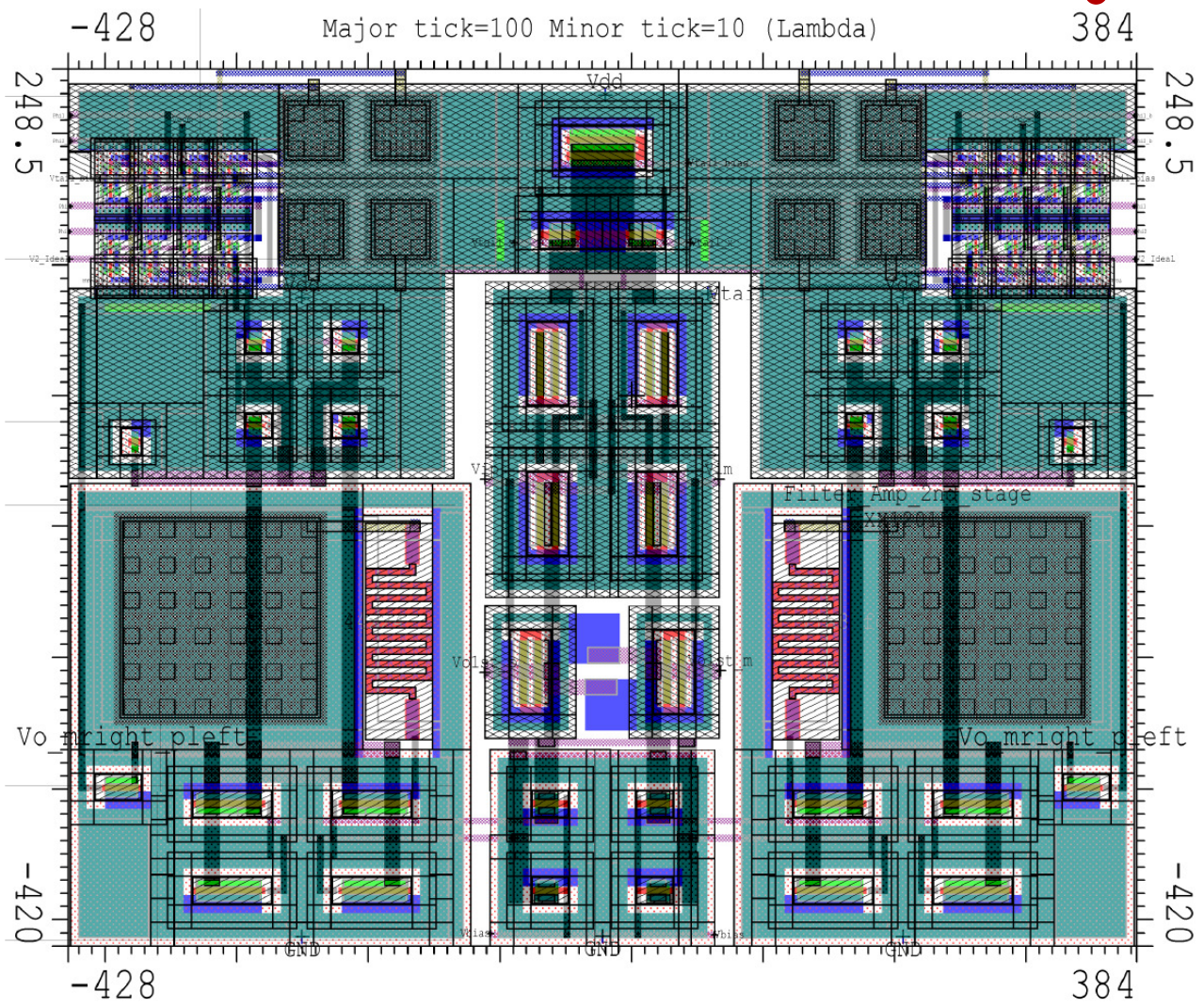
Preliminary layout: Buffer





Preliminary layout: Filter amplifier





Tentative schedule

- July — Finish layout and verification
- August 3rd — The Bean V1.0 tape out
- Oct-Dec — IC tests and measurements

Acknowledgements

We want to thank Ryan Herbst, Lupe Salgado and Mark Freytag for their help in the ADC test setup.

People

- Angel Abusleme (Ph.D. student)
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- Dr. Dietrich Freytag (SLAC)
- Dr. Gunther Haller (SLAC)
- Professor Bruce Wooley (Stanford U.)

Thank you!