OPTIONS FOR THE ATLAS LEVEL-2 TRIGGER

Dick Hubbard / Saclay
for the ATLAS Level-2 Trigger Groups

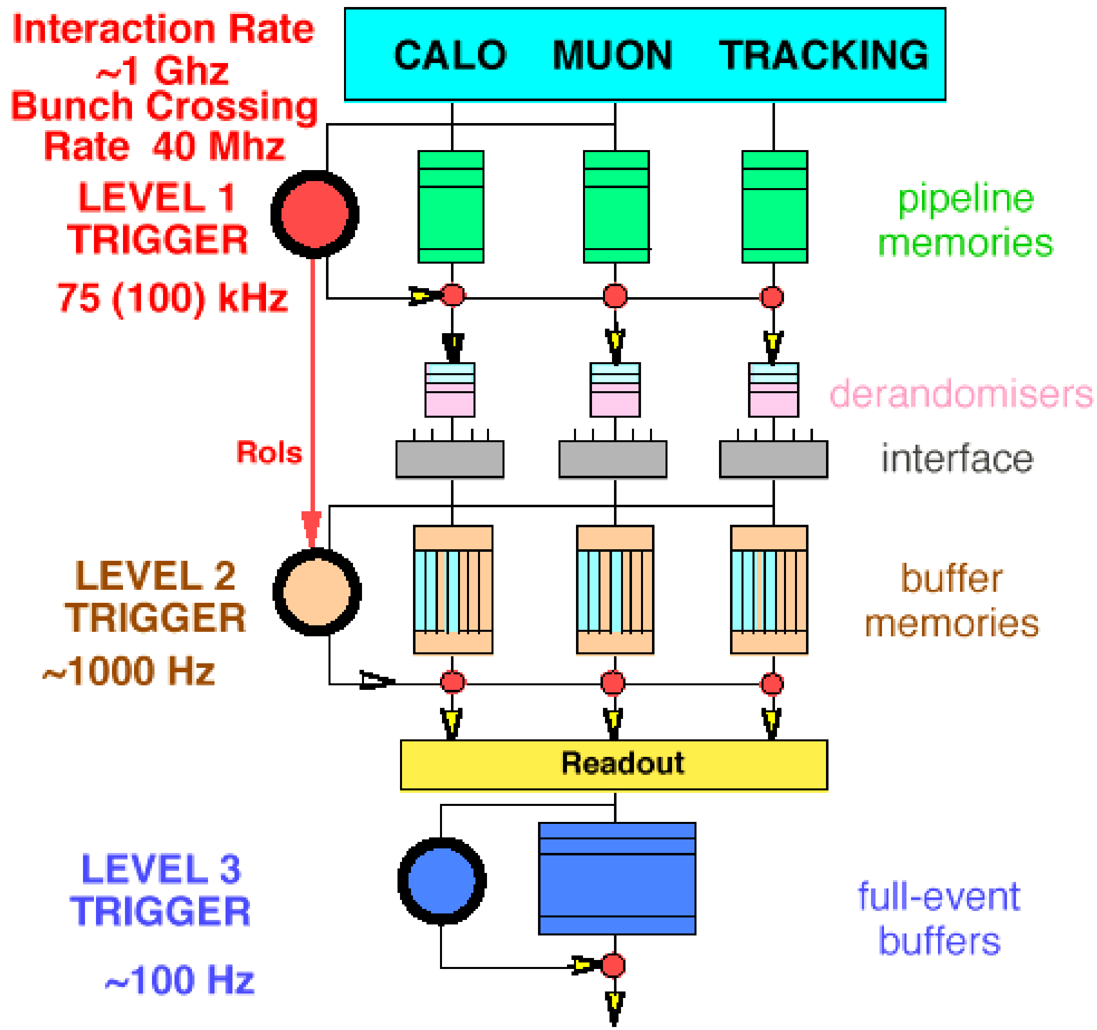
31 institutes
115 physicists and engineers

- **Data flow in the ATLAS trigger/DAQ system**
- **Level-2 trigger architectures**
- **Algorithms at Level 2 and at Level 3**
- **Hybrid architectures with FPGA processors**
- **Emulation and modelling**

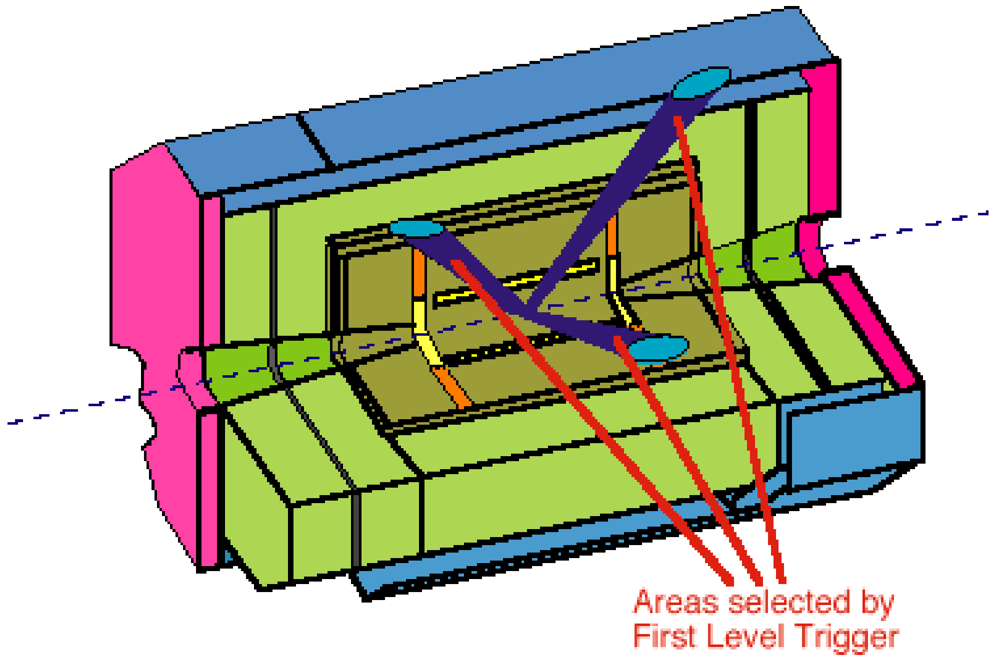
Related talk at CHEP97 by Simon George :

« Performance requirements of proposed ATLAS second level trigger architectures from simple models »

ATLAS Trigger System

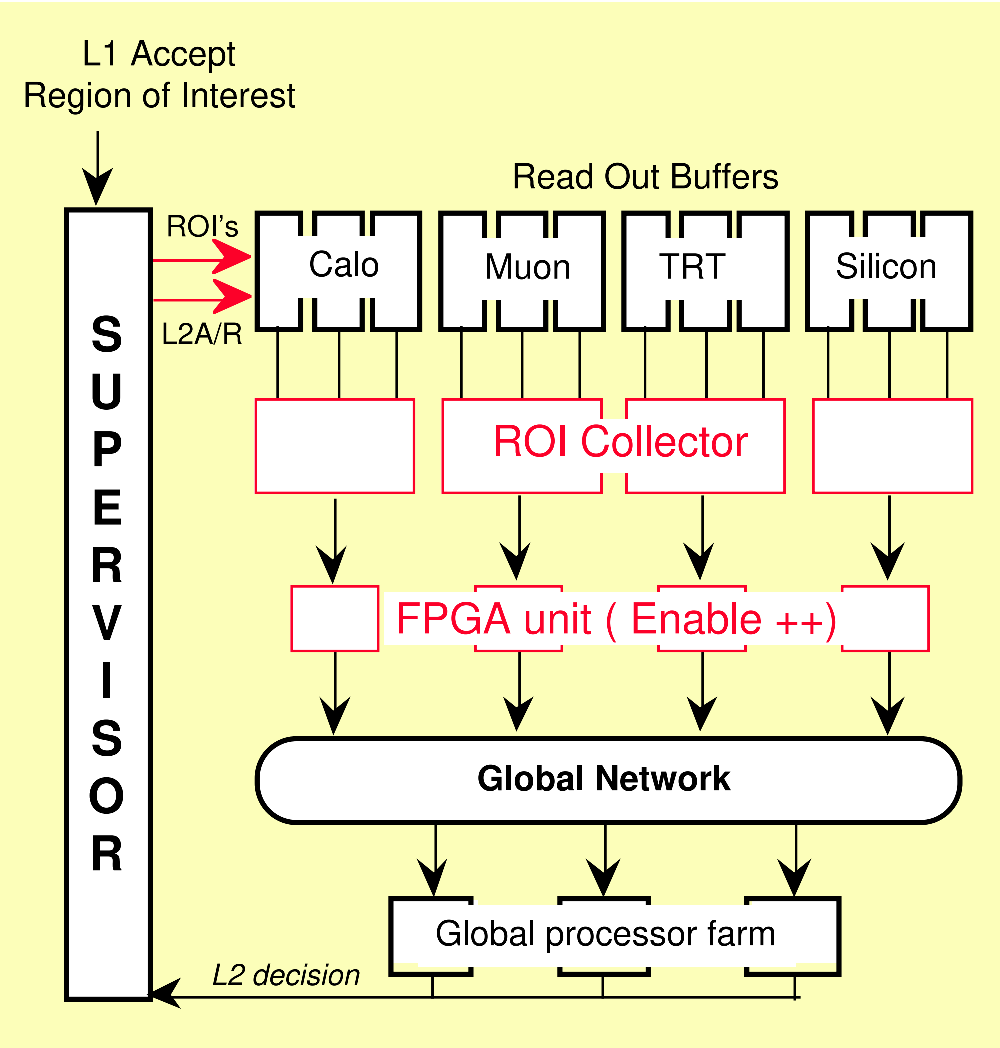


Regions Of Interest



- **Regions of interest identified by Level 1**
- **Average ~ 5 RoIs per event - 1 or 2 pass trigger thresholds**
- **Only RoI data transferred to Level 2 processors**
- **RoI data volume ~ few % of total event data**
- **Level 2 and Level 3 data volumes roughly equal**

Architecture A - FPGA Processors for Feature Extraction



Characteristics :

- FPGA processors - ENABLE ++
- Data-driven - in PUSH mode
- Pipeline step 10 µs
- Global farm of commercial processors

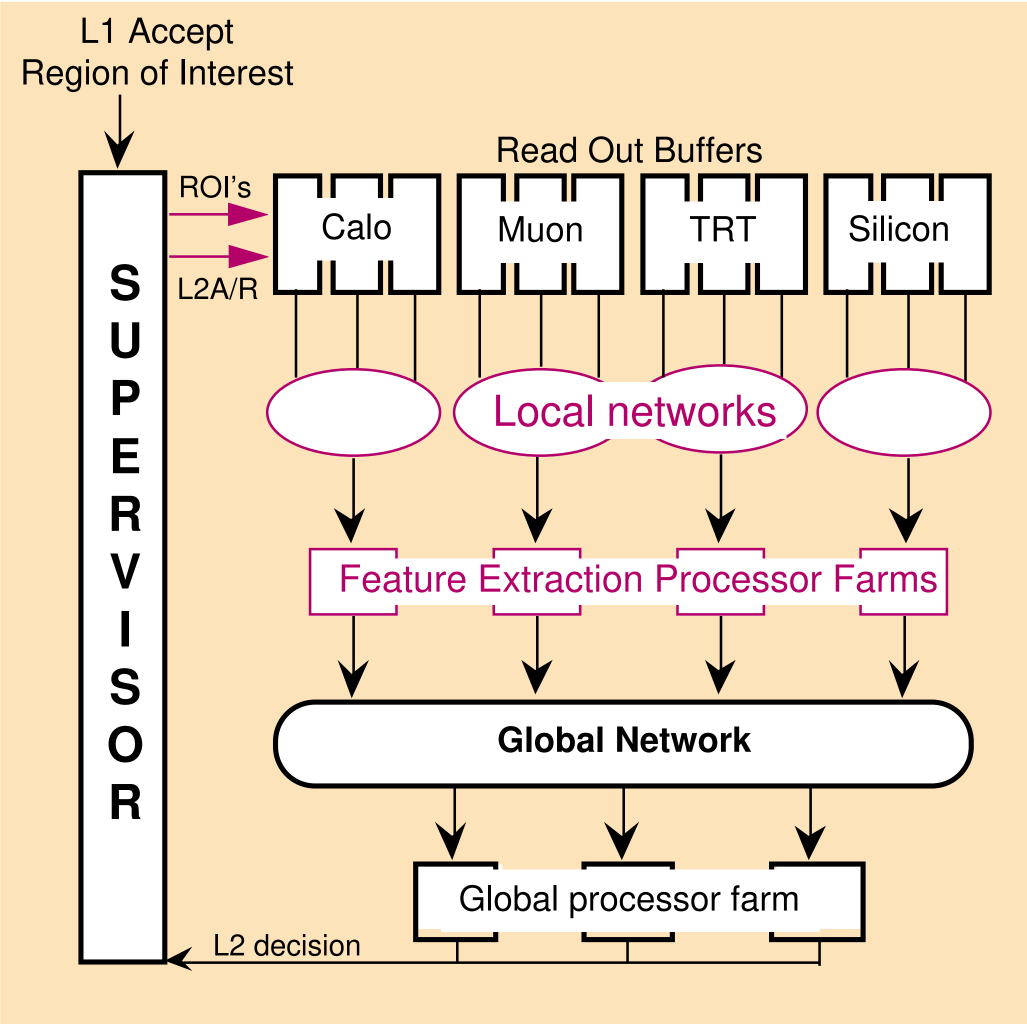
Advantages :

- RoI collection « on the fly »
- Feature extraction at 100 kHz
- Minimal latency

Difficulties :

- RoI collection at 100 kHz
- Limited algorithm complexity
- Sequential processing ruled out

Architecture B - Local / Global Processor Farms



Characteristics :

- ATLAS Technical Proposal design
- Parallel RoI Feature extraction FEX
- Operates in PUSH mode
- Local and global switching networks
- Possibly partition of single network

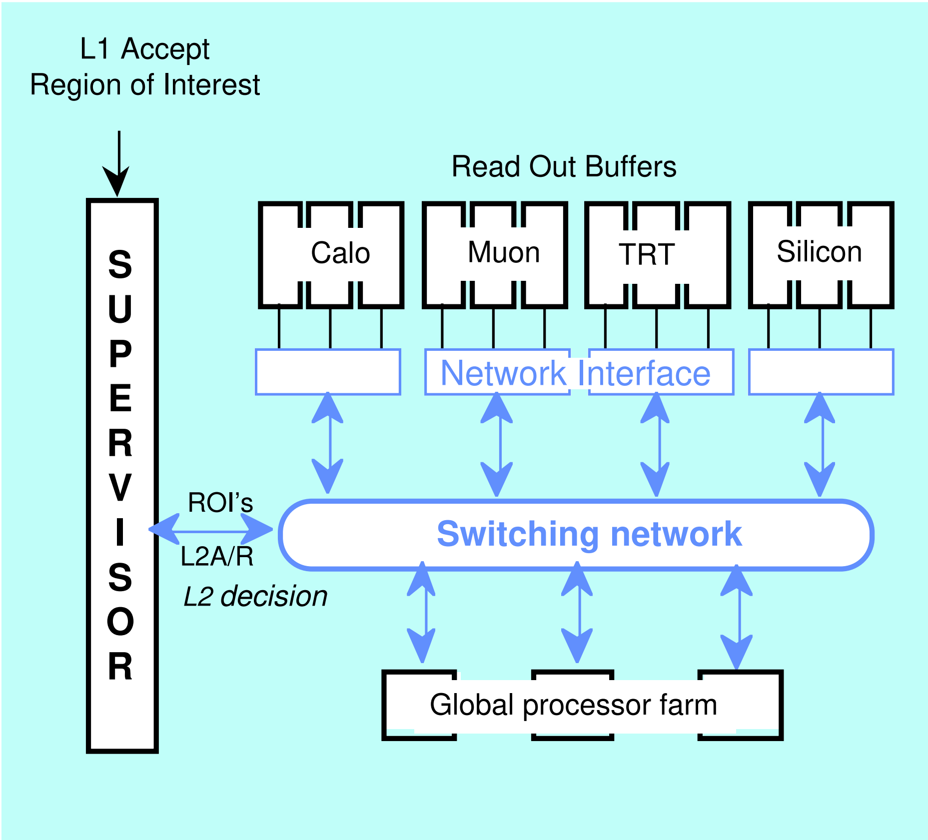
Advantages :

- Reduced latency for parallel FEX

Difficulties :

- Sequential processing complex
- Increased supervisor functionality

Architecture C - Single Processor Farm



Characteristics :

- Optimized for sequential selection
- Single switch, single farm
- Data concentration before switch
- Multiple data requests in PULL mode

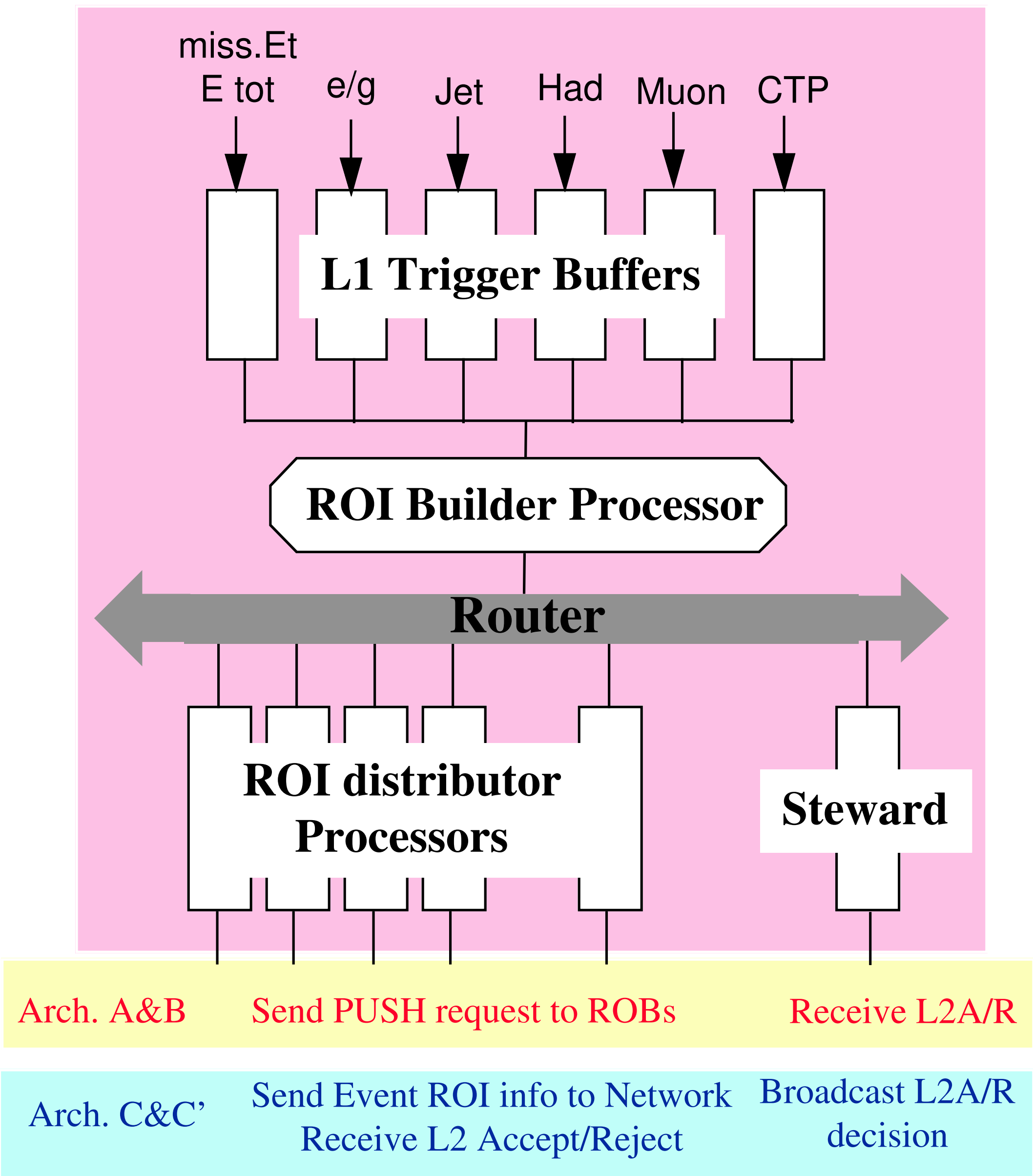
Advantages :

- Well-adapted to sequential processing
- Same architecture as Level 3

Difficulties :

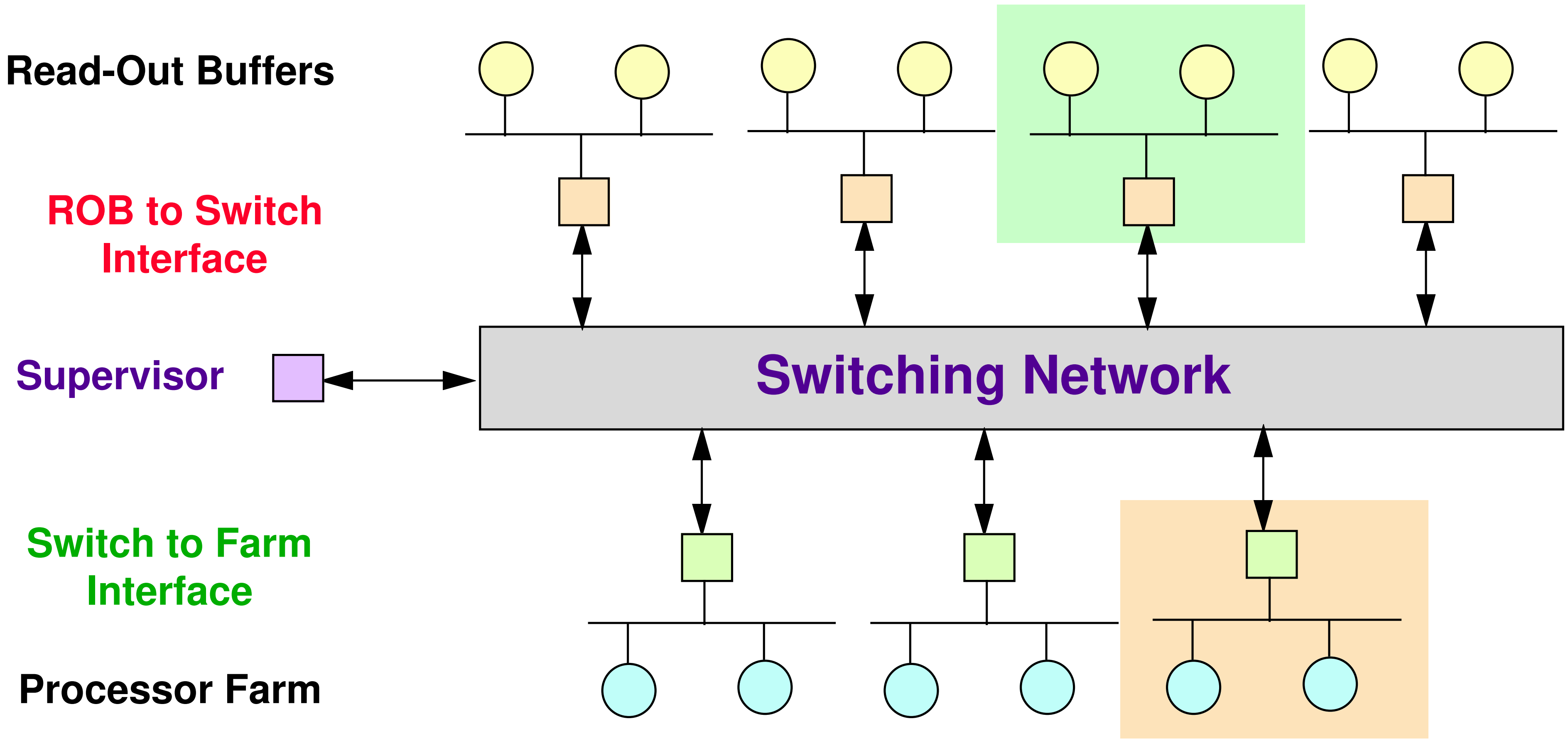
- Data and control traffic on same switch
- Multiple events in each processor

Level 2 Supervisor



- Receives Level 1 Trigger data @100KHz
- Lists ROI type, threshold, η, ϕ
- Assigns processors as needed
- Sends ROI info to ROBs for PUSH
- Sends ROI info to processors for PULL
- Receives / broadcasts L2 decisions
- Data sent to Level 3 if L2 ACCEPT
- Paged memory released in ROBs

Level 2 Data Flow



Algorithms at Level 2 and at Level 3

Trigger must satisfy physics requirements

Loose, redundant triggers
Emphasize flexibility

High-rate Level 1 Regions of Interest (RoIs) **100 KHz**

Dominant at design luminosity $L = 10^{34}$ /cm^2/s

B-physics algorithm @ low luminosity $L = 10^{33}$ /cm^2/s

TRT full scan without RoI guidance $T \sim 50$ ms
Sequential selection algorithm required
FPGA option for higher luminosity $L = 3*10^{33}$ /cm^2/s

B-jet tag algorithm at Level 2 or Level 3

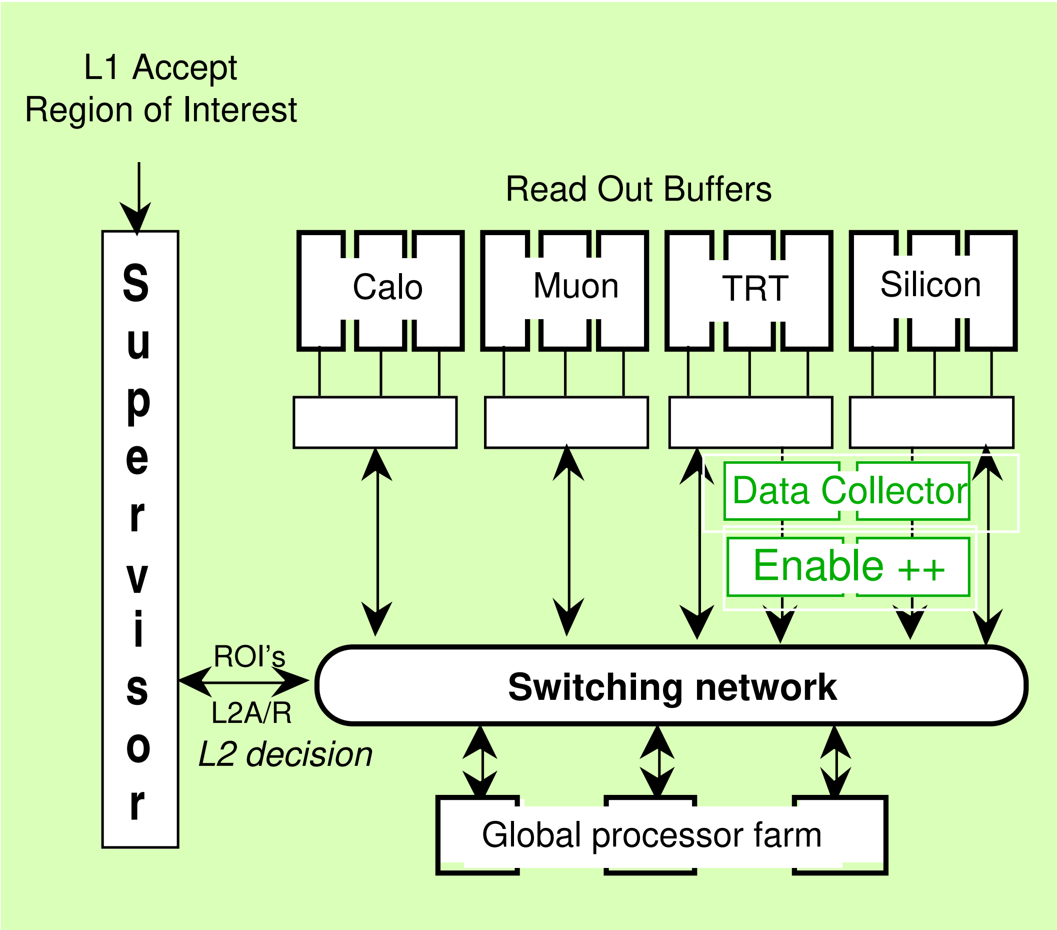
Limited additional data transfer in sequential Level 2
Slower, more precise at Level 3 with full event data

Algorithm Timing and Data Volumes at Level 2

Muon stand-alone algorithm	**100 μs @ 500 MIP**
pattern recognition and P_t	1 kB of data per RoI
Calorimeter cluster finding	**100 μs @ 500 MIPS**
find peak and analyze shape	3 kB for e/γ, 16 kB for jets
Transition Radiation Tracker	**600 μs @ 500 MIPS**
histogram TRT straws	0.3 kB @ $L = 10^{34}$ /cm^2/s
Silicon tracker	**800 μs @ 500 MIPS**
histogram strips and pixels	0.8 kB @ $L = 10^{34}$ /cm^2/s
Full TRT scan for B physics	**50 ms @ 500 MIPS**
find tracks in full volume	16 kB @ $L = 10^{33}$ /cm^2/s
B-jet vertex tag	**250 ms @ 500 MIPS**
find displaced vertex in RoI	3 kB @ $L = 10^{33}$ /cm^2/s

Benchmark on 100 MIPS processor, assume 50 % data handling

Example of Hybrid Architecture - FPGAs for Track Finding



RoI feature extraction as in Arch. C

FPGA processors for TRT full scan

- **Full scan track find in ~ 250 µs**
- **Full scan track fits in 50 ms**

- **Track find for b-jets in ~ 1 ms**
- **Full b-jet tag in ~ 150 ms**

Requires at least one sequential step

Increased trigger flexibility

Expanded physics potential

Enable++ for TRT full scan

B-physics Level-1 trigger **Single μ with $P_t > 6$ Gev/c**

Additional signatures at Level 2 for specific B decay modes

Low-P_t leptons for $B \rightarrow J/\psi + \ldots$
Low-P_t hadrons for $B \rightarrow \pi^+ \pi^-$

Scan full tracking volume for low-P_t tracks - TRT full scan

Time-consuming on standard processor farm ~ 50ms
50% track finding, 50% track fitting

Use FPGA processors ENABLE++ for initial track finding

Parallel Hough transformation ⇒ histograms
All tracks $P_t > 0.5$ GeV/c ⇒ 30 000 channels
Pipelined access to Look-Up-Table
Full scan execution on 2 boards in 250 μs

24 highly-complex FPGAs per board
12 Mbyte fast SRAM for LUT implementation
Can be scaled up and reconfigured as needed

Emulation and Modelling

Demonstrators measure technological limits of critical systems

- Processor allocation
- Multi-task operation
- Data collection
- Switch performance

Emulators verify scalability

- MACRAME is a 1024-node DS-link emulator
- Architectures Bb and C can be emulated
- Demonstrators can be incorporated in the emulator

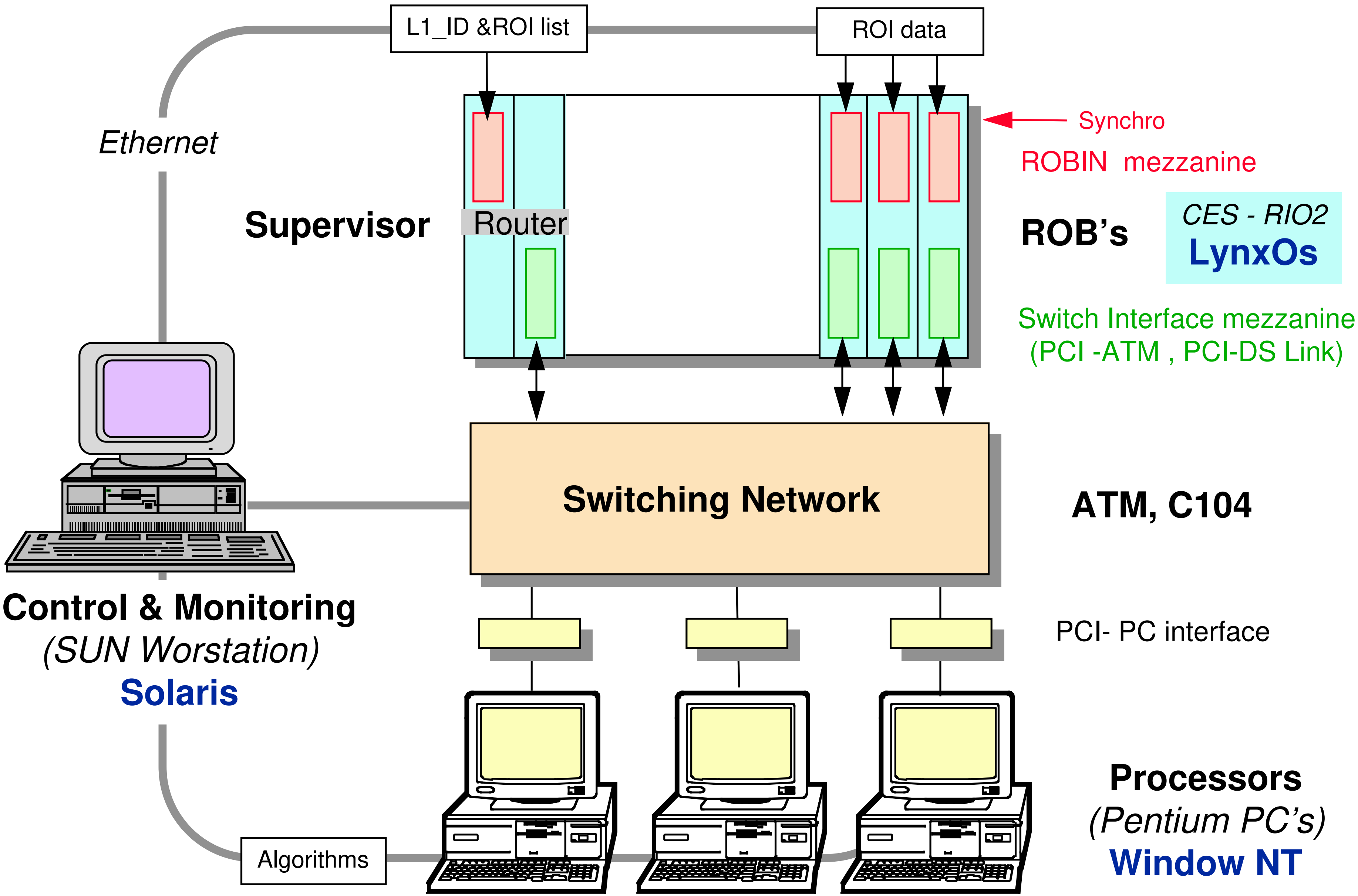
Paper models find initial design parameters Talk by S. George

- Simplified model based on full trigger menus
- Queueing not included in paper models
- Switching network congestion is ignored

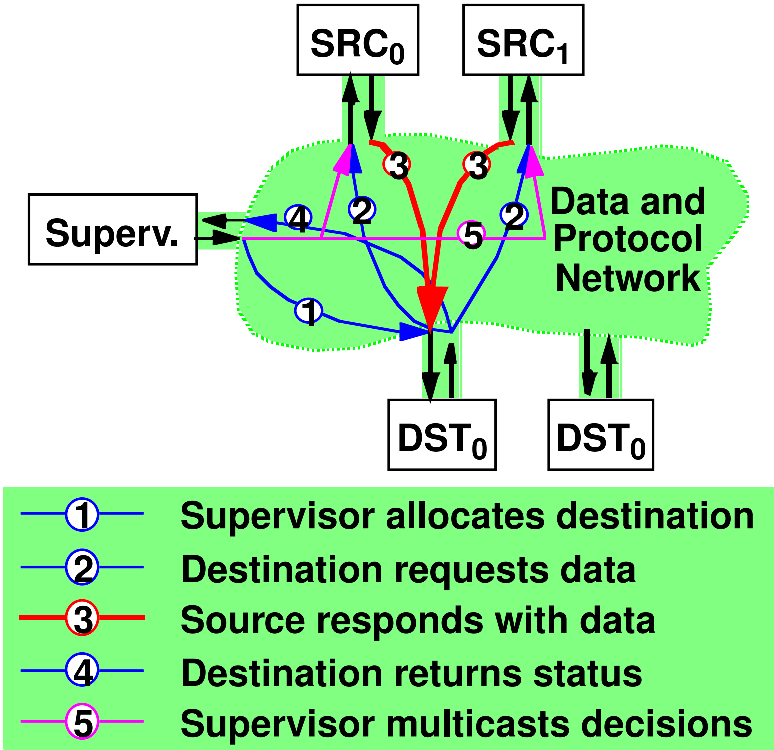
Computer models determine final system performance

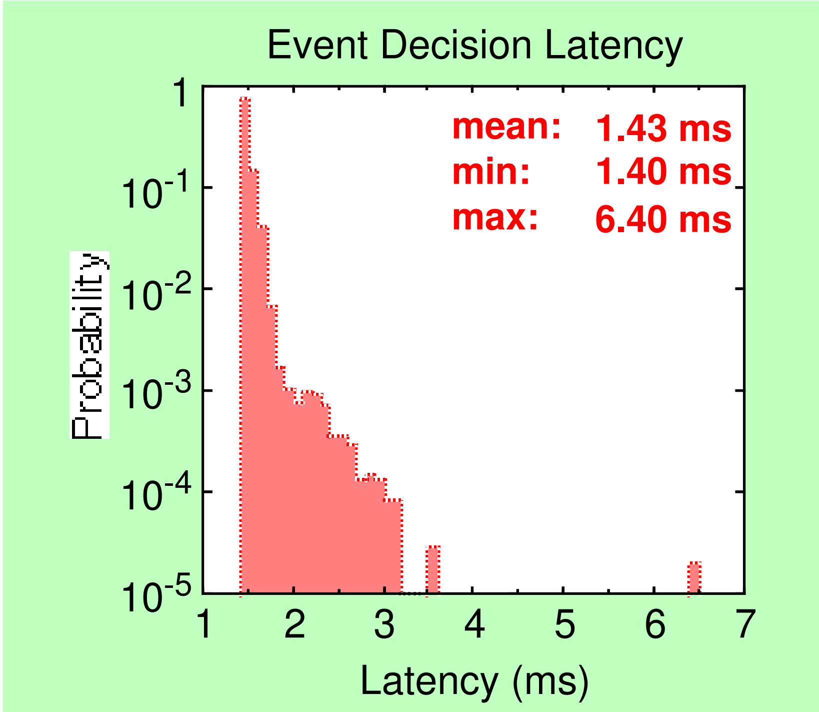
- Initial parameters from paper models
- Initial timing based on average values
- Final results based on GEANT data files

Demonstrator for Architecture C



Measurements on demonstrator C





Final Remarks

ATLAS has a wide program of study to evaluate Level 2 options

- **PUSH or PULL data flow architecture**
- **Separate or combined data and control networks**
- **Parallel and sequential processing options**
- **Data collection systems and network interfaces**
- **Processor sub-farm interfaces and control**

The Level 2 and Level 3 programs are interdependent

Several families of commercial products under study

- **ATM, DS-link, and SCI switching networks**