Calorimeter trigger electronics for CMS detector at LHC

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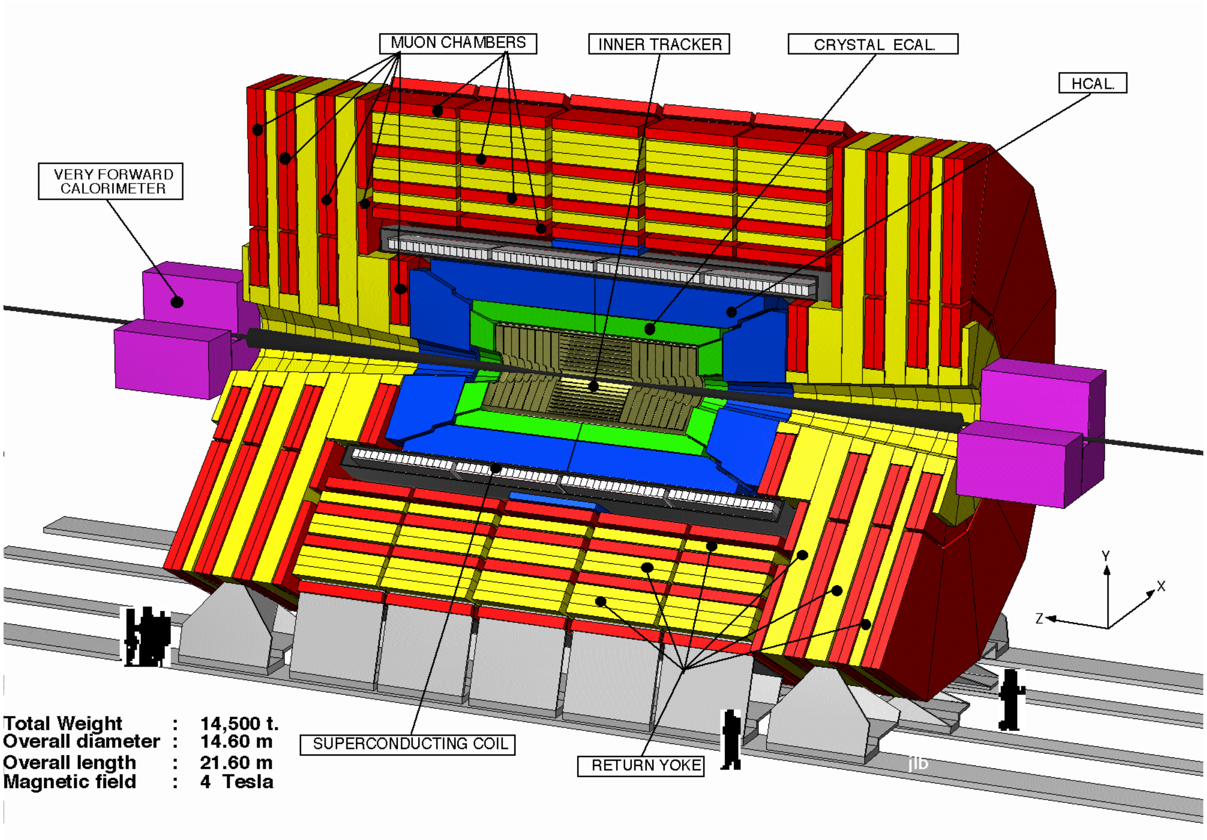
CMS trigger/DAQ system overview
Trigger algorithms
Implementation of calorimeter trigger
Prototype efforts
Physics performance

CMS Trigger/DAQ Problem

A Compact Solenoidal Detector for LHC



CMS LHCC Meeting, 19 January 1995 Overview 2

Detector	Channels	Occupancy%	Event size (kB)	Level-1
Pixel	80000000	.01	100	No
InnerTracker	16000000	3	700	No
Preshower	512000	10	50	No
Calorimeters	125000	5	50	Yes
Muons	1000000	.1	10	Yes

LHC Crossing frequency	40 MHz
LHC Luminosity	10^{34} cm^{-2} s^{-1}
Minimum bias interaction rate	25 * 40 MHz = 10^9 Hz
Rate of hard interactions with leptons/photons	100 Hz
Archival capacity in 2005	100 Hz (10^7 reduction)

Solution: Use calorimeter and muon data to identify upto 100 kHz of potentially interesting events with high P_t electrons, photons, muons, jets and neutrinos in custom built trigger electronics within 3 μs. Filter out 100 Hz of truly interesting events after online analysis with conventional algorithms on commercial CPUs.

CMS/LHC Physics

Standard model Higgs (high luminosity)

- H (80 GeV) $\rightarrow \gamma\gamma$
- H (120 GeV) $\rightarrow$ Z Z* (4 leptons)
- H (>500 GeV) $\rightarrow$ leptons (+ ν's)
- H (< $2M_W$ Associated t or W or Z) $\rightarrow$ b b (lepton + X)

SUSY Higgs (low luminosity)

- (standard model Higgs like channels)
- h, H, A $\rightarrow \tau\,\tau$ (lepton + X)
- A $\rightarrow$ Z h ; h $\rightarrow$ bb (lepton + X)
- p p $\rightarrow$ t t X; t $\rightarrow H^+$ b; $H^+ \rightarrow \tau\,\nu$; t $\rightarrow$ lepton + X

SUSY sparticle searches (low luminosity)

- MSSM sparticle $\rightarrow$ LSP (Missing E_t) + n jets
- MSSM sparticle $\rightarrow$ Same sign dileptons + X

Other new particles

- Z' $\rightarrow$ dileptons
- Leptoquarks: dileptons

Top physics (low luminosity)

- t $\rightarrow$ lepton + X
- t $\rightarrow$ multijets

Bottom physics (low luminosity)

- b $\rightarrow$ lepton + X
- b $\rightarrow \psi k_s$ (leptons + X)

QCD

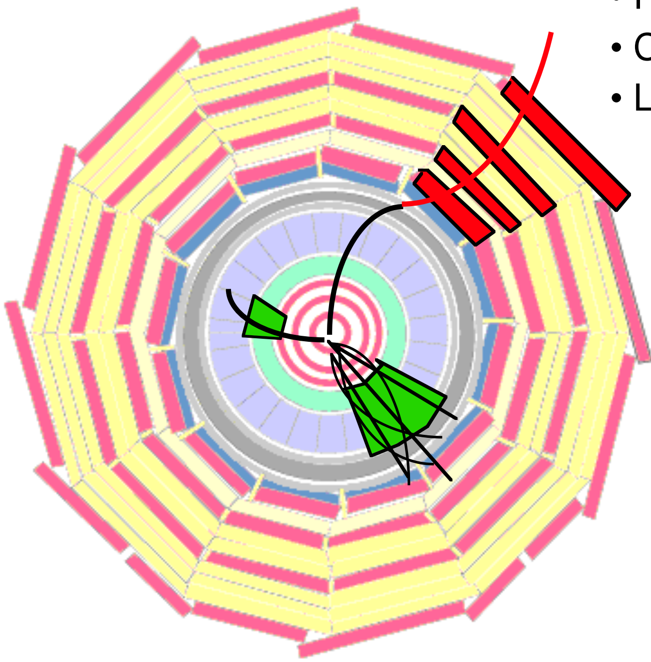
- Low luminosity 100 GeV jets
- High luminosity 200 GeV jets

Trigger candidates:

- High luminosity: lepton/γ (30 GeV), dileptons/$\gamma\gamma$ (15 GeV)
  missing E_t (100 GeV), jets (200 GeV)
- Low luminosity: lepton/γ (15 GeV), dileptons/$\gamma\gamma$ (10 GeV)
  missing E_t (50 GeV), jets (100 GeV)

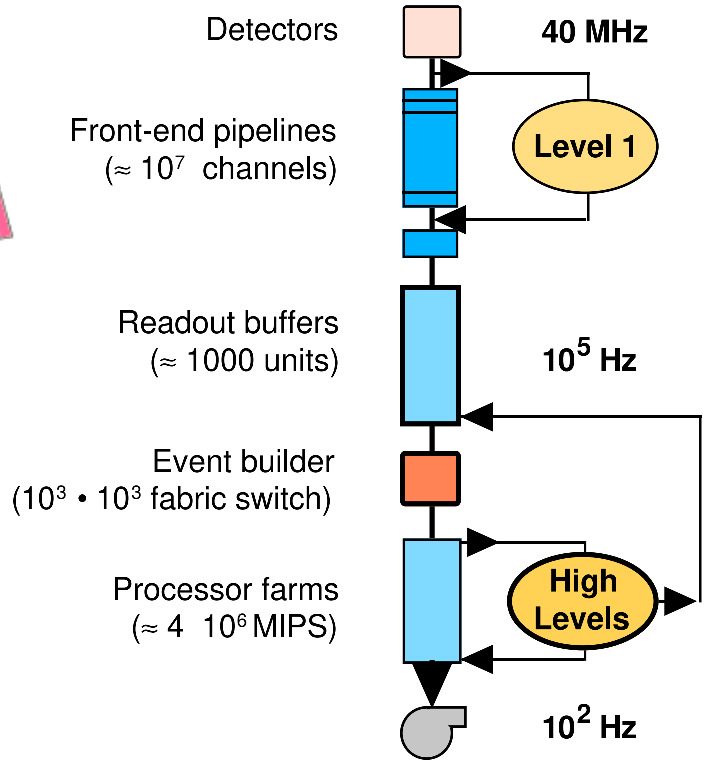
CMS Trigger Levels

40 MHz

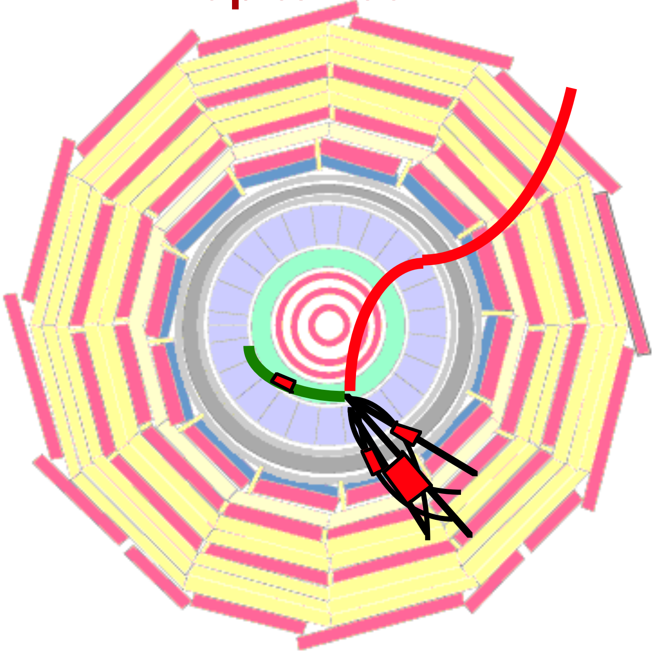


Level-1. Specialized processors

- Particle ID: electron/γ, muon, jets, missing E_T
- Coarse granularity to reduce data volume
- Local pattern recognition and energy sums

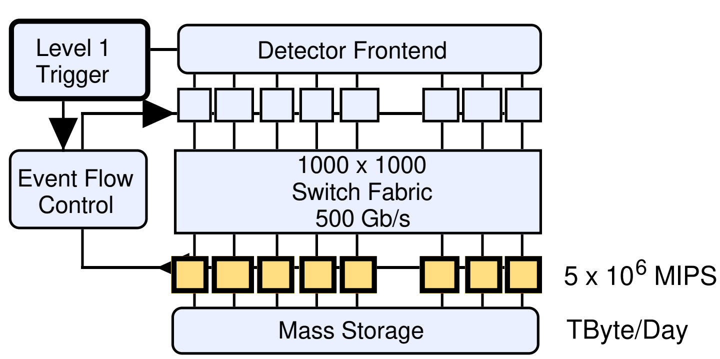


up to 100 kHz



High trigger levels. CPU farms

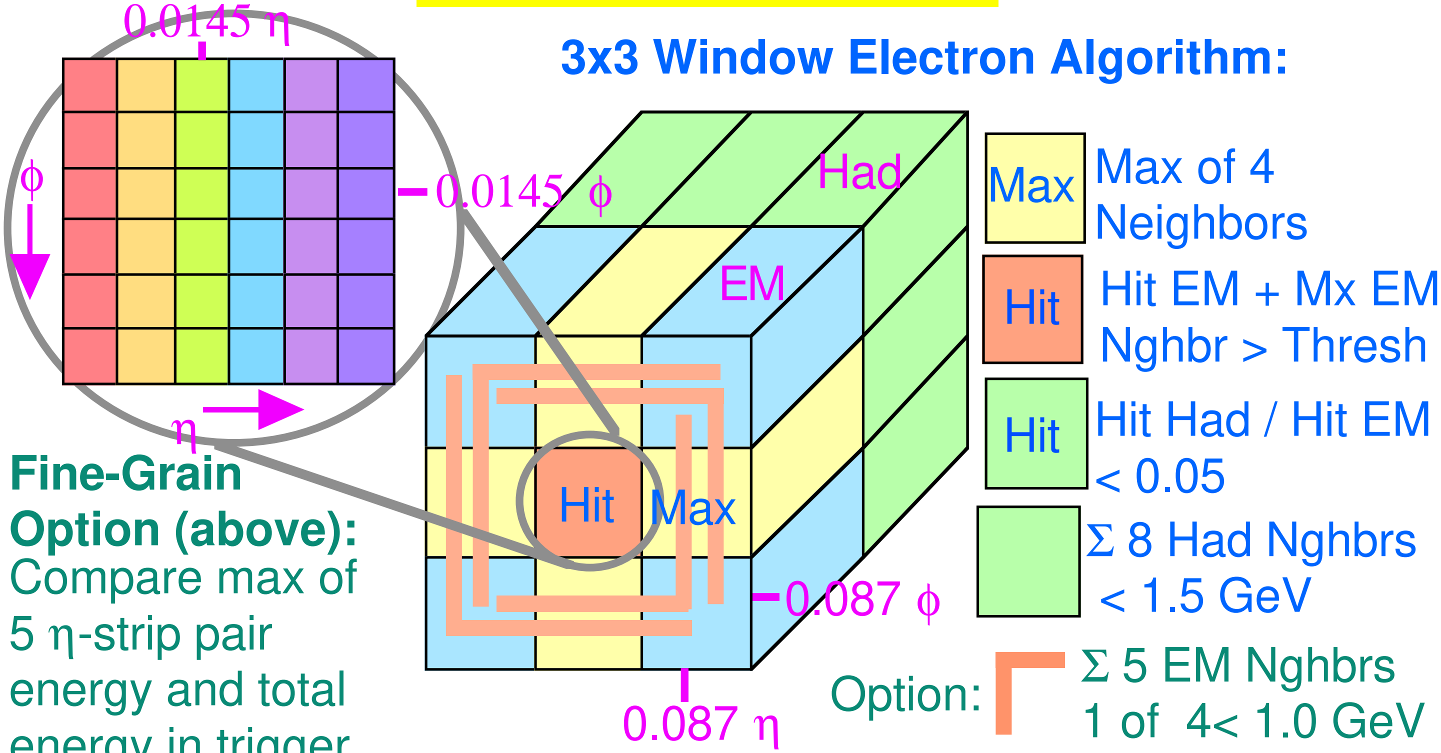
- Clean particle signature (Z, W, quarks..)
- Finer granularity precise measurement
- Kinematics. Effective mass cuts and topology
- Track reconstruction and detector matching
- Event reconstruction and analysis



≈ 100 Hz

Calorimeter trigger algorithms

Electron/Photon trigger



Fine-Grain Option (above): Compare max of 5 η-strip pair energy and total energy in trigger tower.

Tower count = 72φ x 54η x 2 = 7776

Jet trigger

4 x 4 non-overlapping trigger tower sums, i.e., 0.348φ x 0.348η

Missing energy trigger

E_x, E_y calculated from 4 x 4 sums and added to obtain missing E_t

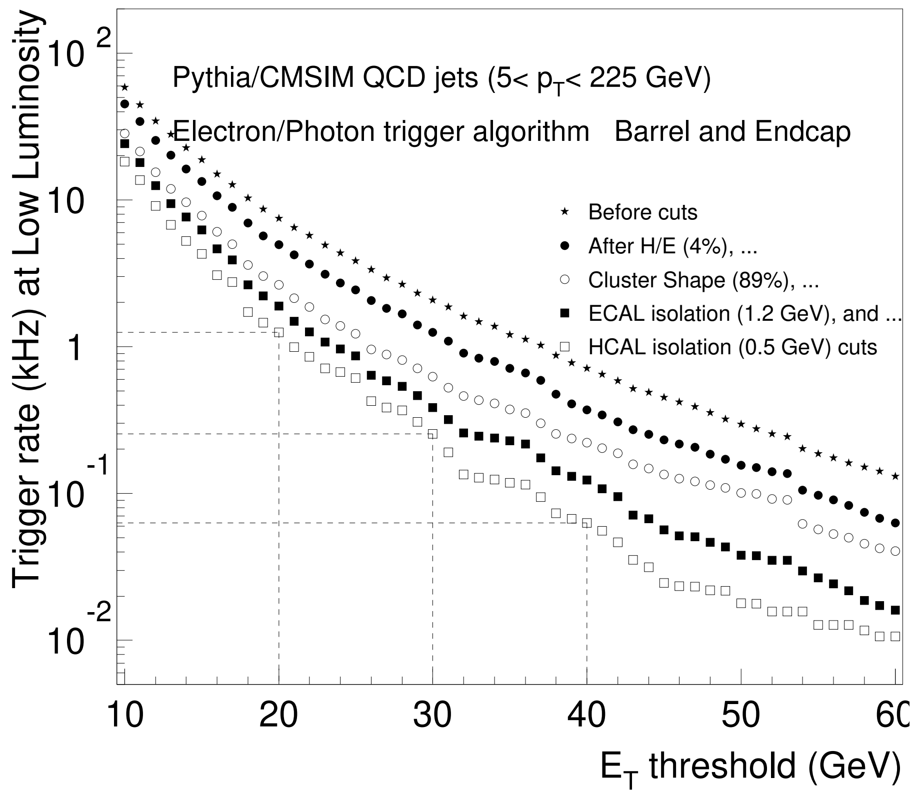
Benefits of multi-cut EM algorithm

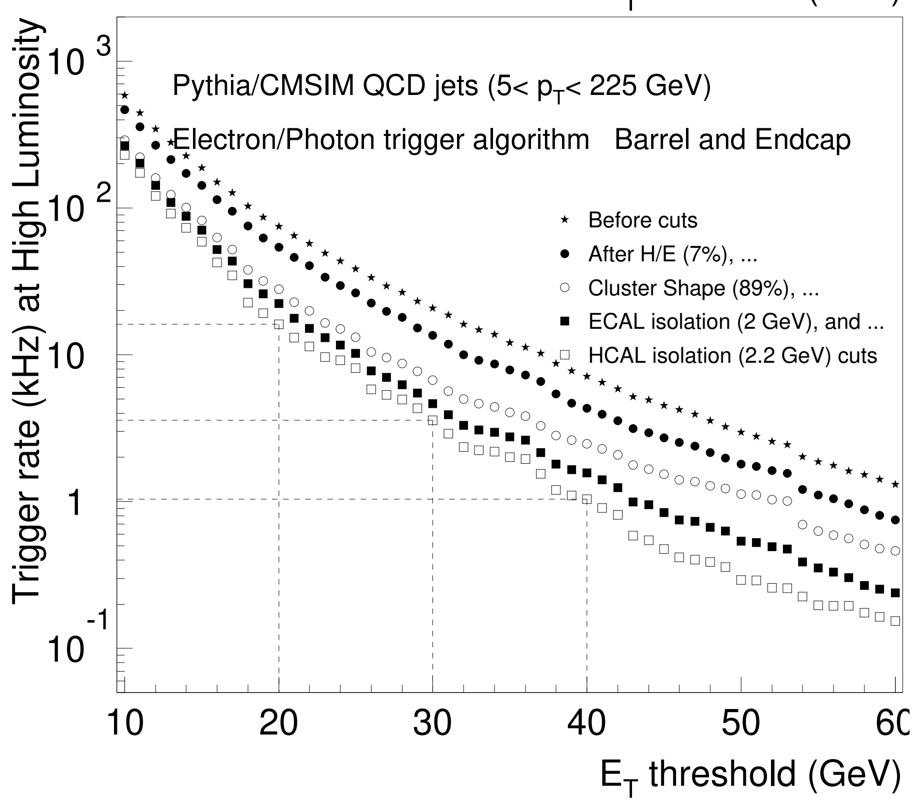
Low luminosity

- **Use H/E and fine-grain EM cluster shape cuts to provide "non-isolated" electron/γ trigger to emphasize top and B physics.**

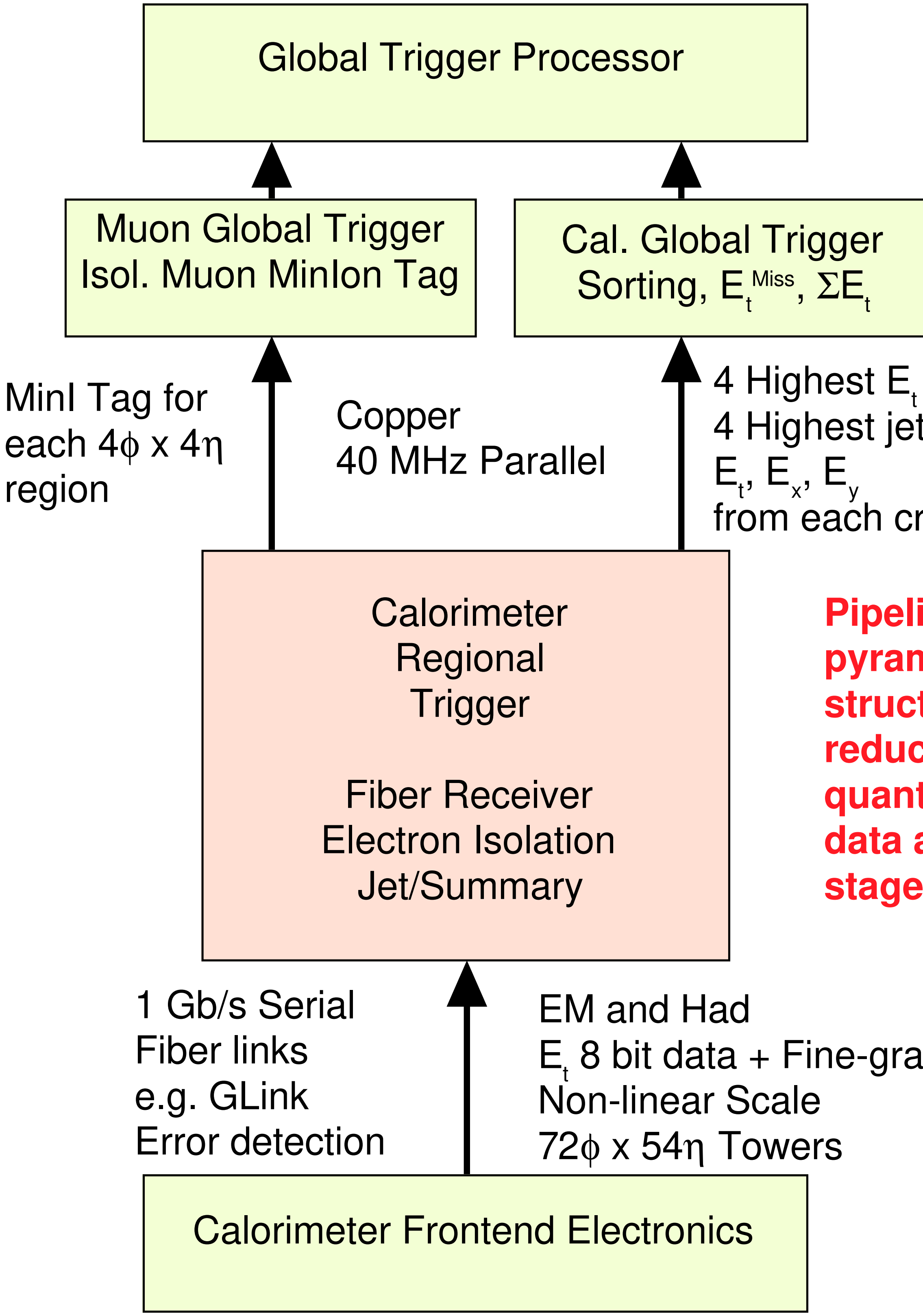
High luminosity

- **Use additional ECAL and HCAL isolation to further cut background rate to provide high P_t electron/γ trigger for electro-weak physics.**
- **Continue to provide "non-isolated" electron/photon trigger, albeit pre-scaled, to provide top and B physics samples.**





Level-1 Trigger Data Flow Chart



Pipelined pyramidical structure reduces quantity of data at each stage.

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Front-end: Trigger primitives

ECAL Crystal or HCAL tower data tapped off at 10-bit resolution for forming trigger primitives while full resolution data is placed in the pipeline

No data sharing between trigger towers

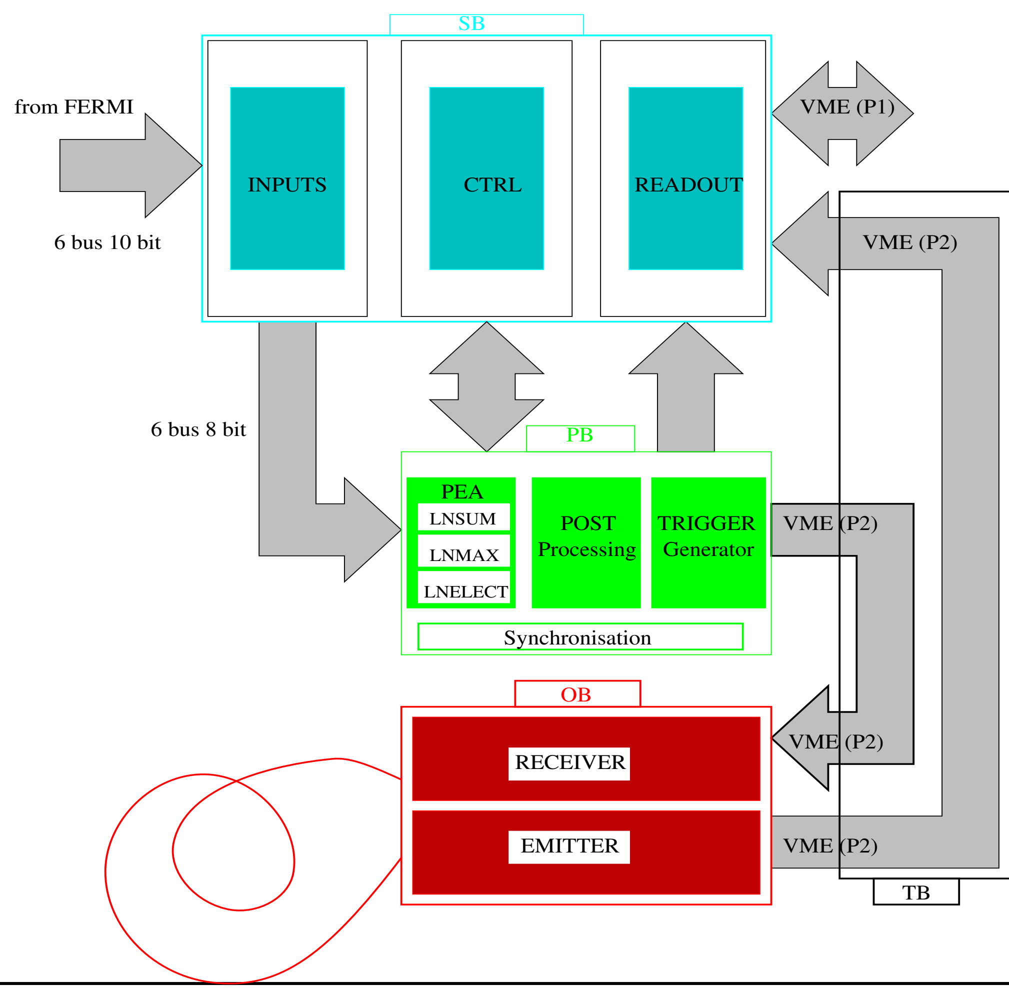
Calculates and Outputs on fiber to regional system

- ECAL: Sum E_t in the trigger tower and fine-grain bit
- HCAL: Sum E_t and HAC1 / HAC2 comparison bit

Prototype tests to verify ECAL fine-grain concept

Initial ECAL prototype tests used four boards

Synoptic TPB
(SB, PB, OB, TB)

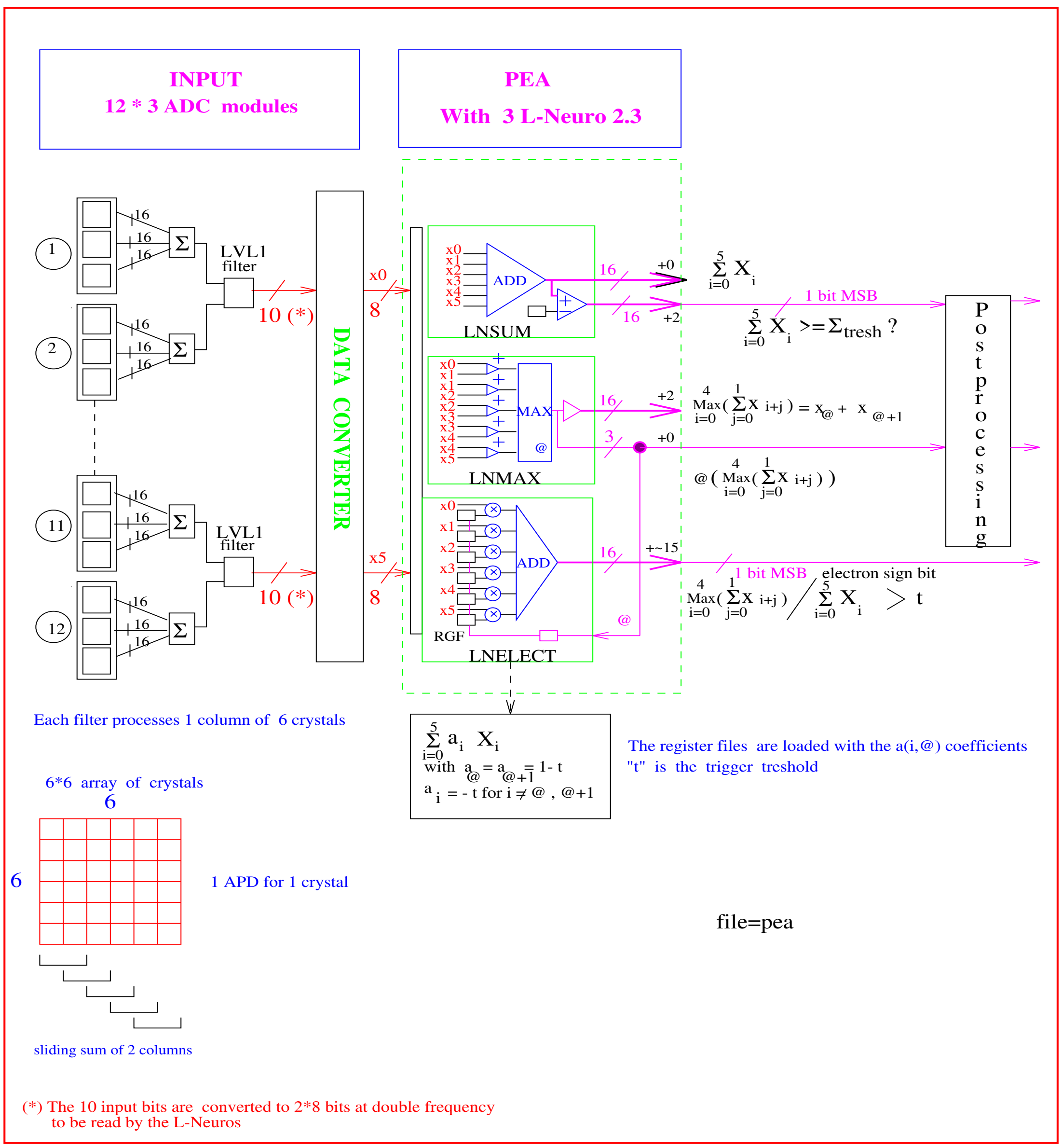


Primitives Extraction ASIC

Prototype PEA board used three previously built L-Neuro II ASICs to calculate the overlapping pair sums and the total E_t, and to identify the maximum pair.

Design elements from the L-Neuro will be used to build a new ASIC which incorporates all the features of ECAL fine-grain algorithm.

PRIMITIVES EXTRACTOR ASIC (PEA)

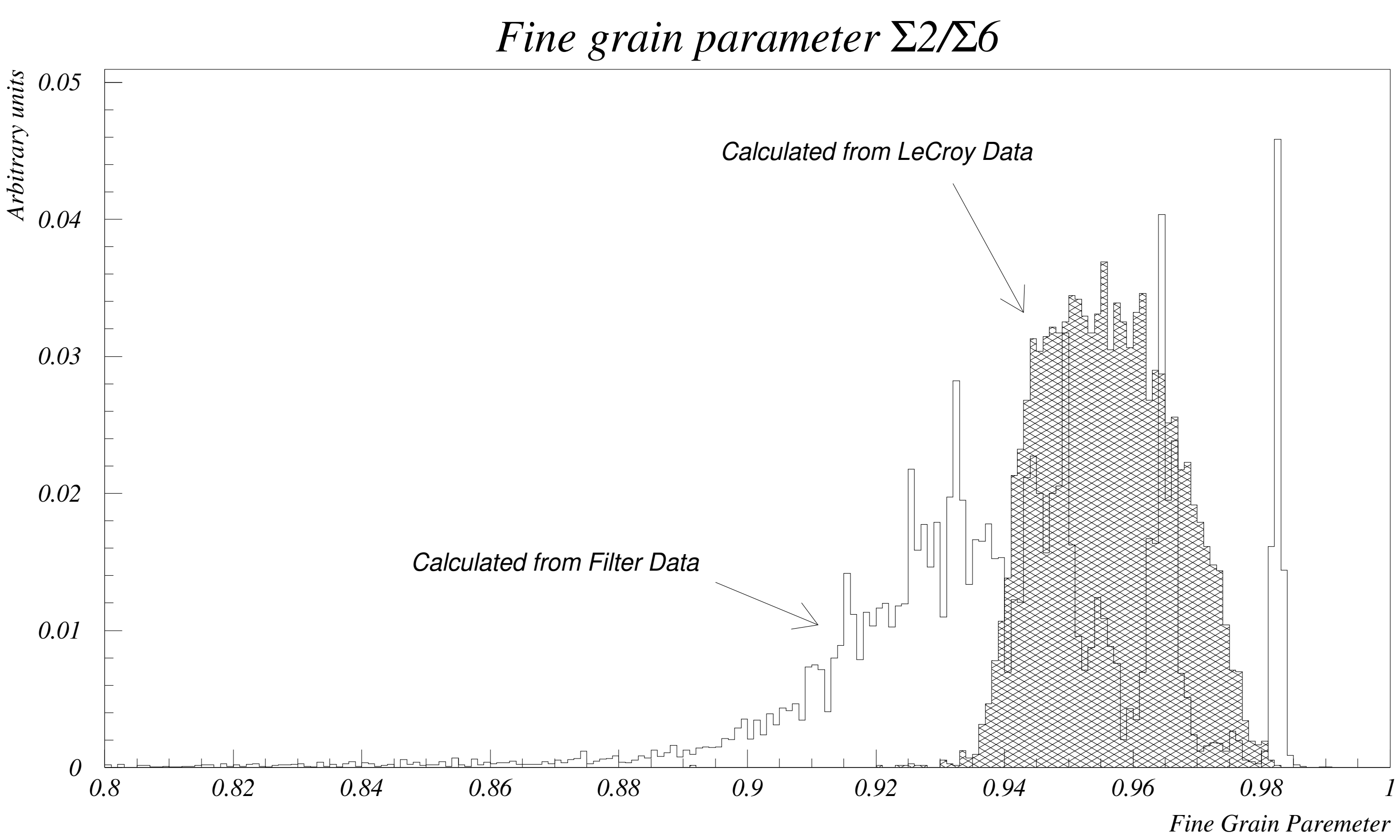


Fine-grain: Test beam results

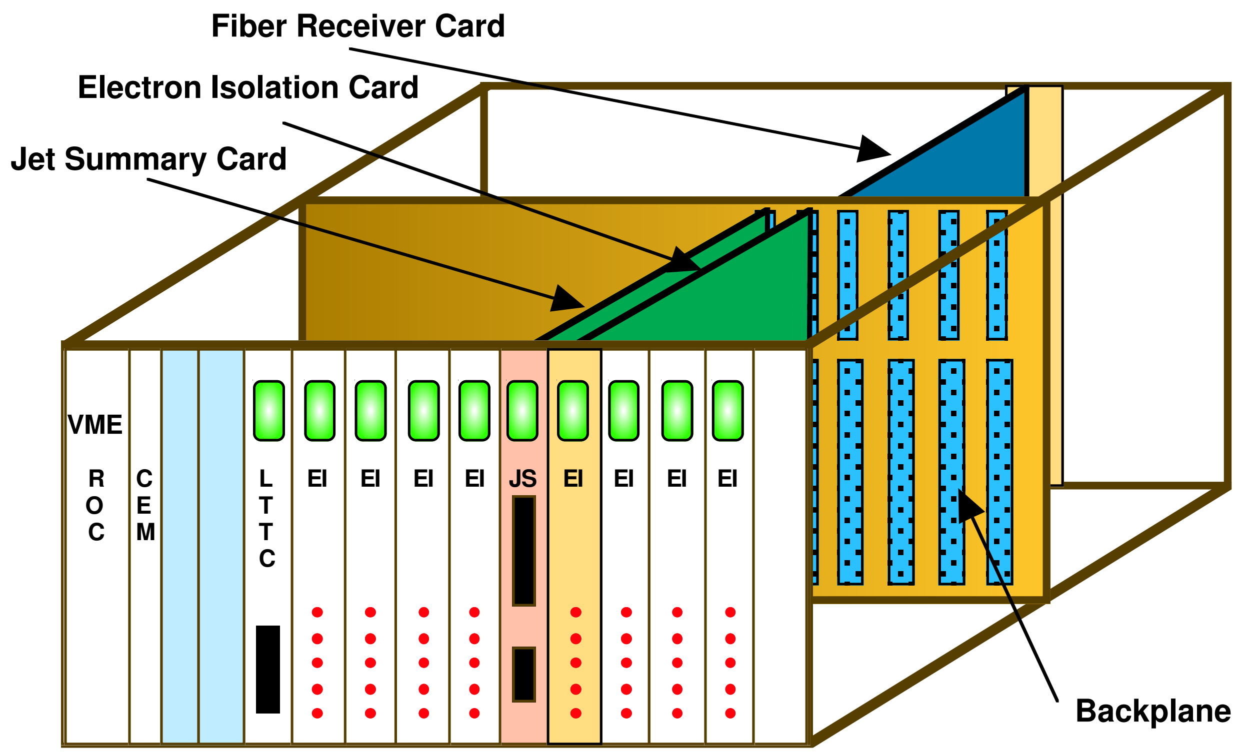
The system operated well in test beam.

Allowed studies of linearity of filters used to obtain energy deposits in a crossing.

The fine-grain parameter determined experimentally shows that electrons can be identified with high efficiency.



Calorimeter regional trigger crate



Data from calorimeter FE on optical fibers

- Into rear-mounted Receiver Cards

160 MHz point to point backplane

- Receiver, Electron Isolation, Jet Summary Cards Operate @ 160 MHz

Output to calorimeter global trigger

- From Jet Summary Card

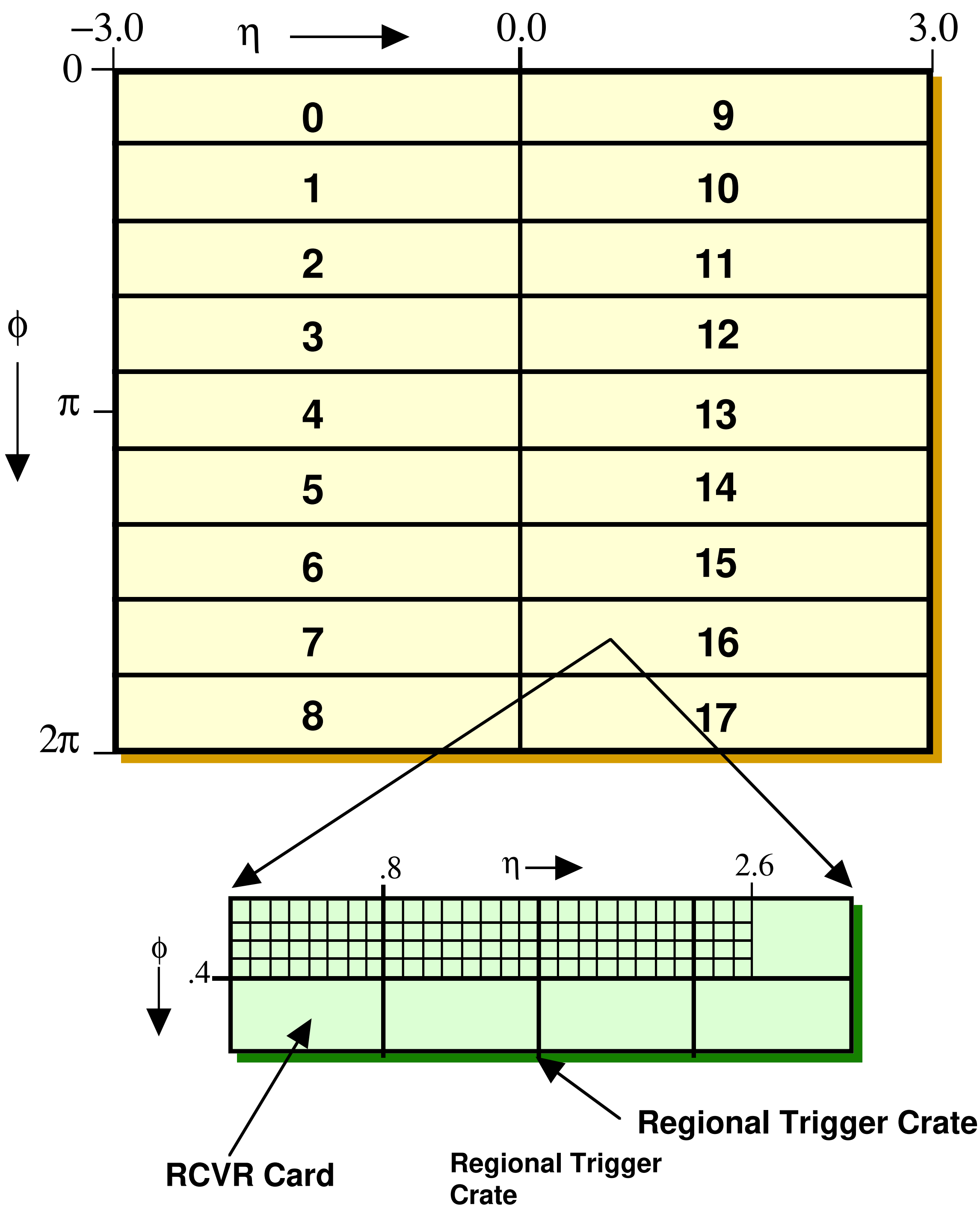
Min Ion and Quiet bits to muon trigger

Conceptual design

- Identified components & characteristics
- Considered system integration issues (mechanics, power distribution, cooling ...)

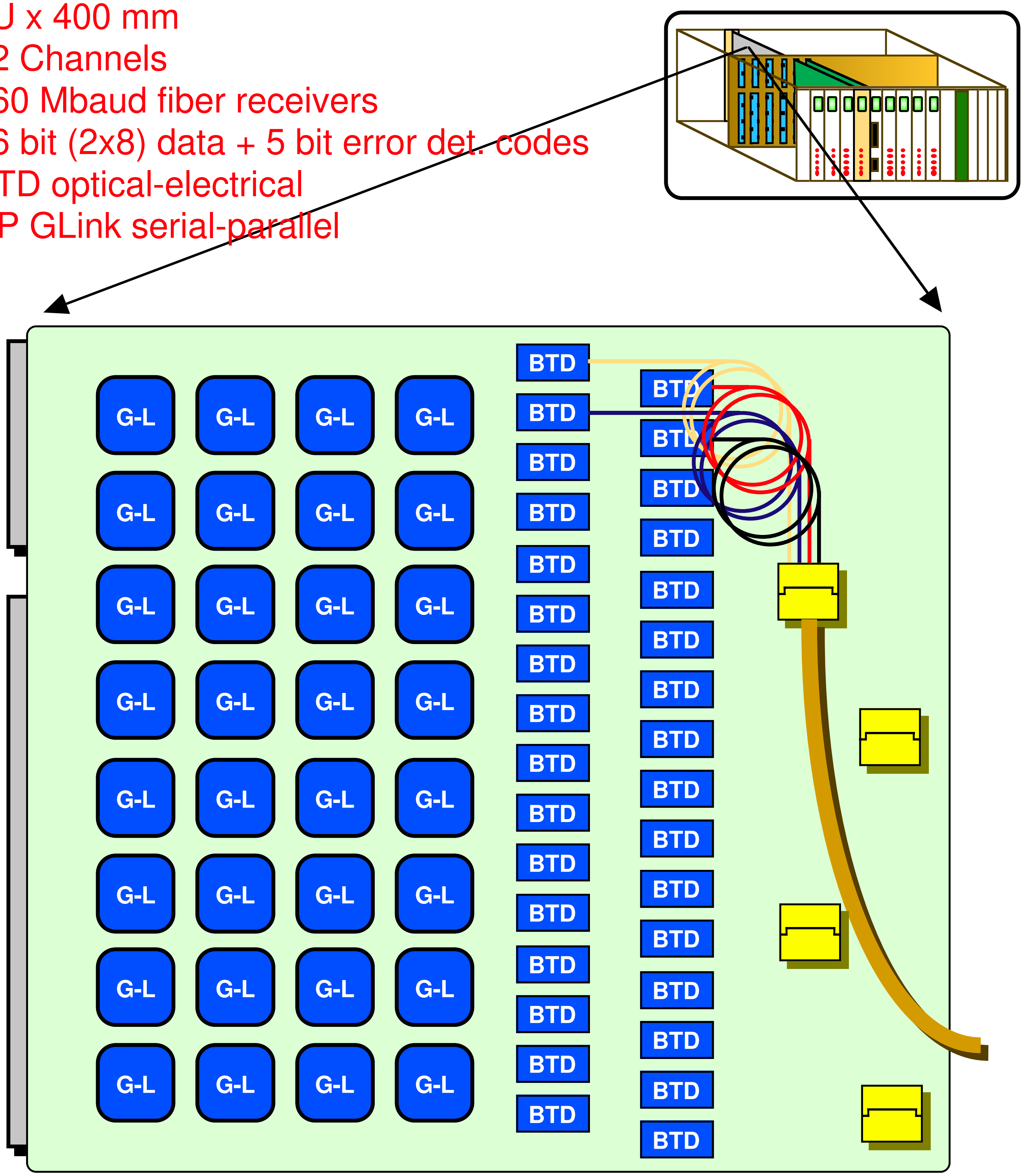
Calorimeter mapping

18 crates for full calorimeter
Each crate processes 8x27 region - 40 'spare' channels
Each Receiver/Isolation card pair covers one 4x8 region

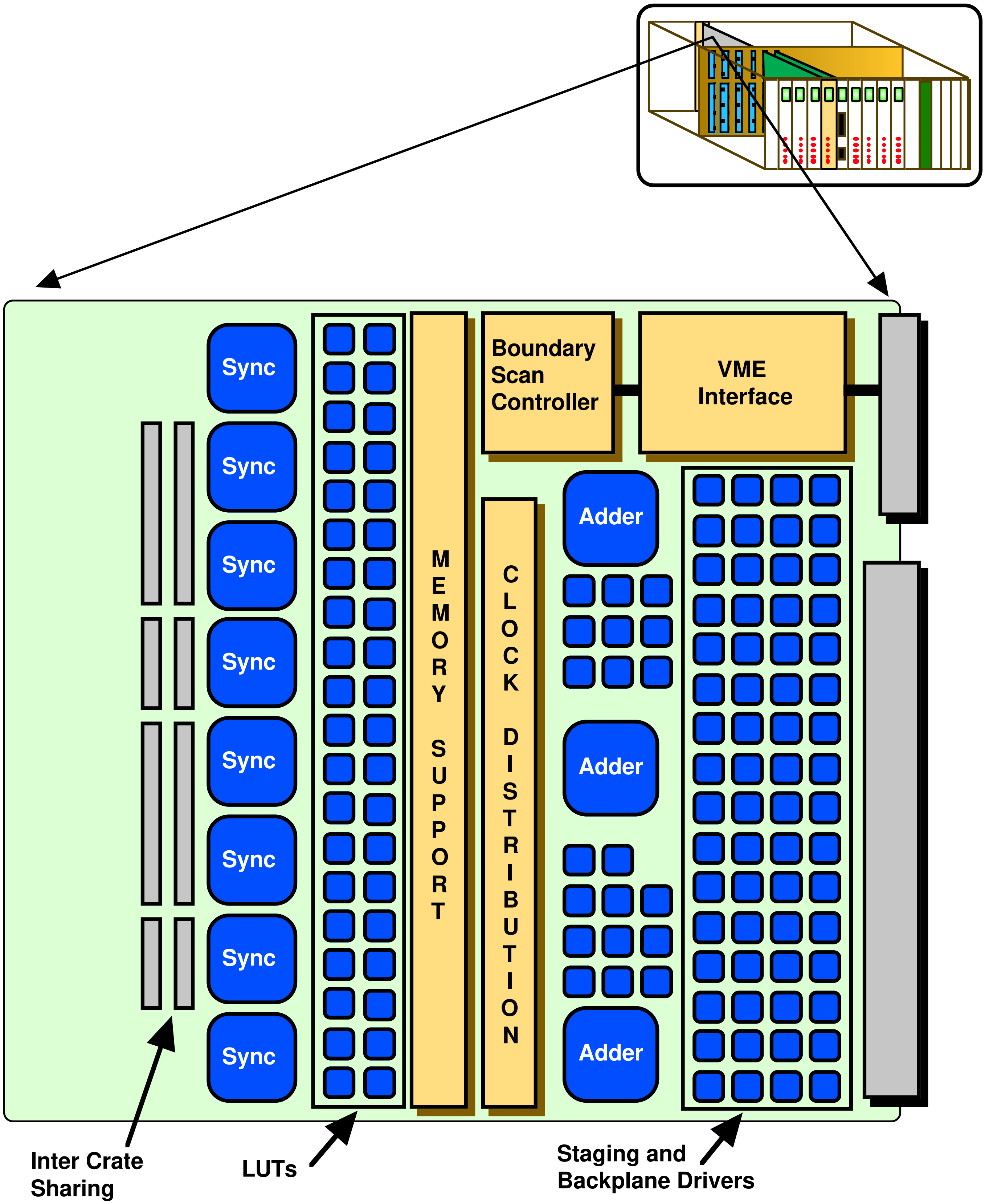


Fiber Receiver Card - Rear

9U x 400 mm
32 Channels
960 Mbaud fiber receivers
16 bit (2x8) data + 5 bit error det. codes
BTD optical-electrical
HP GLink serial-parallel



Fiber Receiver Card - Front



Fiber Receiver Card - Front

Data received from rear side

Data Synchronization

- Each Sync ASIC handles four detector channels
  - Two HAD or two EM inputs, with error detection, per channel @ 40 MHz
  - Four HAD and four EM outputs, with error bits, on two ports @ 160 MHz
- Synchronization method is fully developed
- Technology for this chip has not been chosen

Memory Lookup Tables

- Data handled at 160 MHz
- Presently considering a Quad-Linear scale
- Not limited to any particular encoding

Adder Tree

- Each ASIC handles 8 operands @ 160 MHz
- Two ASICs are at the top of the tree
- One ASIC at the bottom produces E_T for two 4 x 4 regions

Output Staging

- Packed for efficient use by the Electron Isolation Logic
- Data is transmitted differentially at 160 MHz via 340 signal AMP stripline connector
- Intercrate data is transmitted at 80 MHz
- Backplane data is buffered to compensate for intercrate communication time

Error Logic

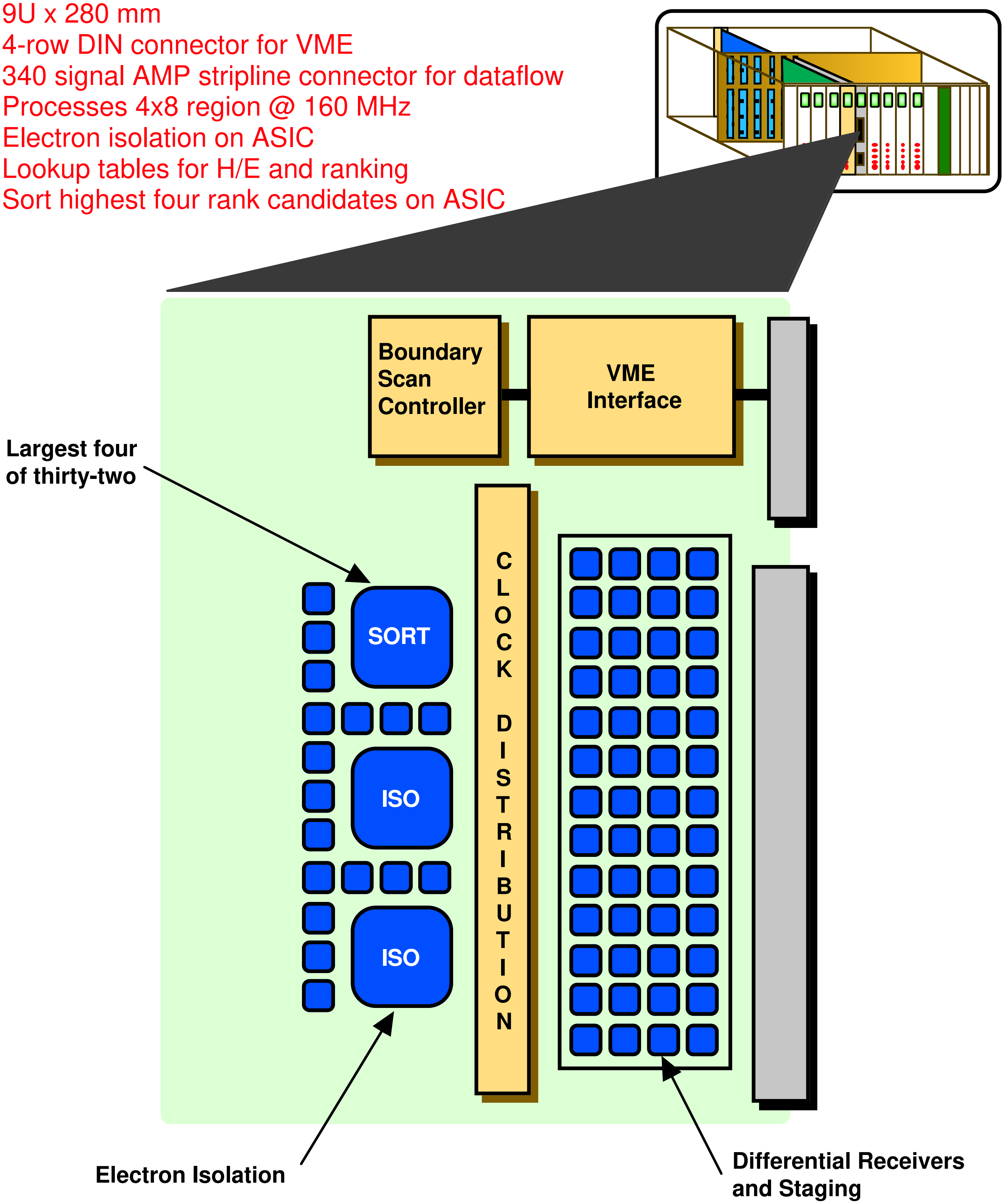
- One error bit per 4 x 4 region forwarded with Adder Tree data
- Errors are stored and histogrammed by channel

Full boundary scan logic

VME control on 4-row DIN

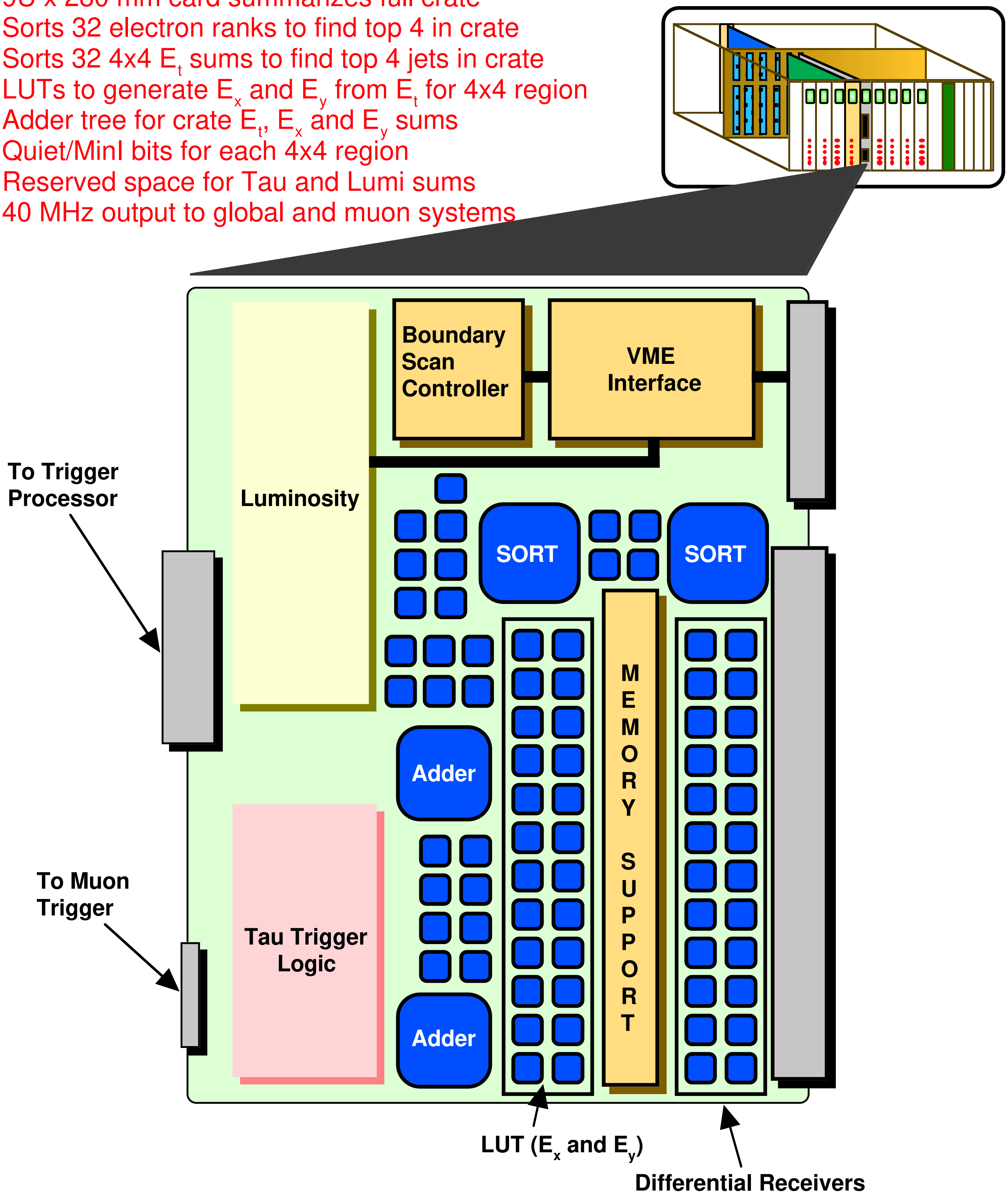
Electron Isolation Card

9U x 280 mm
4-row DIN connector for VME
340 signal AMP stripline connector for dataflow
Processes 4x8 region @ 160 MHz
Electron isolation on ASIC
Lookup tables for H/E and ranking
Sort highest four rank candidates on ASIC



Jet/Summary Card

9U x 280 mm card summarizes full crate
Sorts 32 electron ranks to find top 4 in crate
Sorts 32 4x4 E_t sums to find top 4 jets in crate
LUTs to generate E_x and E_y from E_t for 4x4 region
Adder tree for crate E_t, E_x and E_y sums
Quiet/MinI bits for each 4x4 region
Reserved space for Tau and Lumi sums
40 MHz output to global and muon systems



Latency

Receiver Card, After Sync – .5 crossings

- 1/4 crossing in LUT
- 1/4 crossing to board output

Backplane – .25 crossings

- 1/4 crossing

Electron Isolation Card – 5.75 crossings

- 1/4 crossing to first stage of Isolation chip
- 1/4 crossing to second stage of Isolation chip
- 1/4 crossing to third stage of Isolation chip
- 1/4 crossing to 4-way compare in Isolation chip
- 1/2 crossing to output of Isolation chip
- 4 crossings in Sort chip
- 1/4 crossing to buffer output to next card

Backplane – .25 crossings

- 1/4 crossing

Jet Summary Card – 4.5 crossings

- 4 Crossings in Sort chip
- 1/2 crossing to stage data for output connector

Total: 11.25 crossings

Regional Trigger Prototype effort

Backplane Prototype

- Full size design with all positions routed
- Completed fabrication
- Assembled in a crate

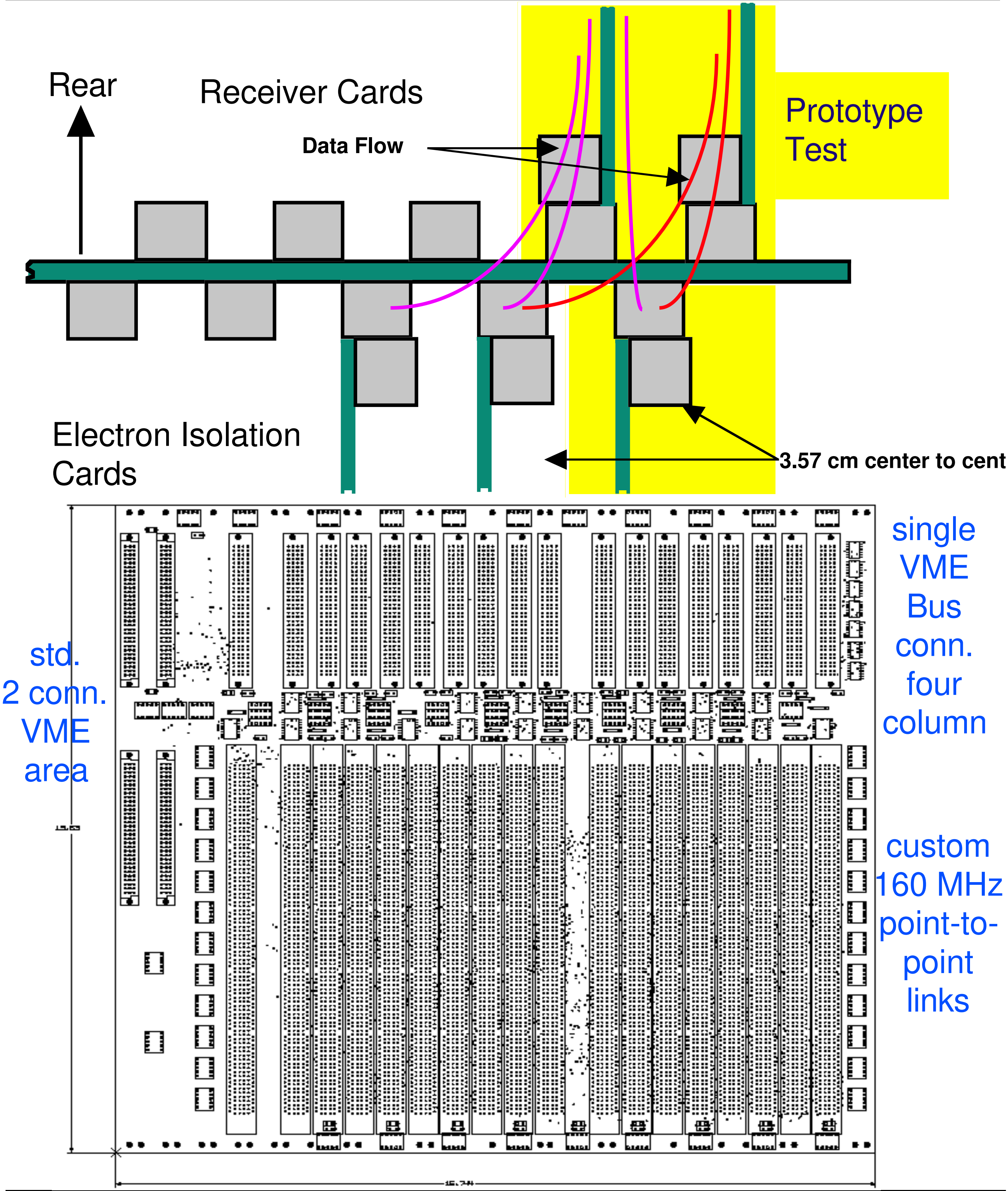
Test crate

- Goals
  - Prove feasibility of 160 MHz data flow
  - Confirm mechanical integrity of the system
  - Examine timing and ground offset problems
- Test cards
  - Two primitive Receiver cards
  - One Electron Isolation card
  - Simple clock card in LTTC position
    - Built and tested
    - Initial tests indicate good clock quality (<1ns rise time) at farthest point on the backplane
  - Commercial VME control station

ASIC Tester

- Being implemented as a stripped down Receiver Card
- Memory Lookup Tables supply test vectors at 160 MHz
- A JTAG controller tests the ASIC's JTAG and some board level boundary scan techniques
- Driver - Connector - Backplane integrity test
- Board level Clock distribution concept verification

160 MHz Backplane Layout



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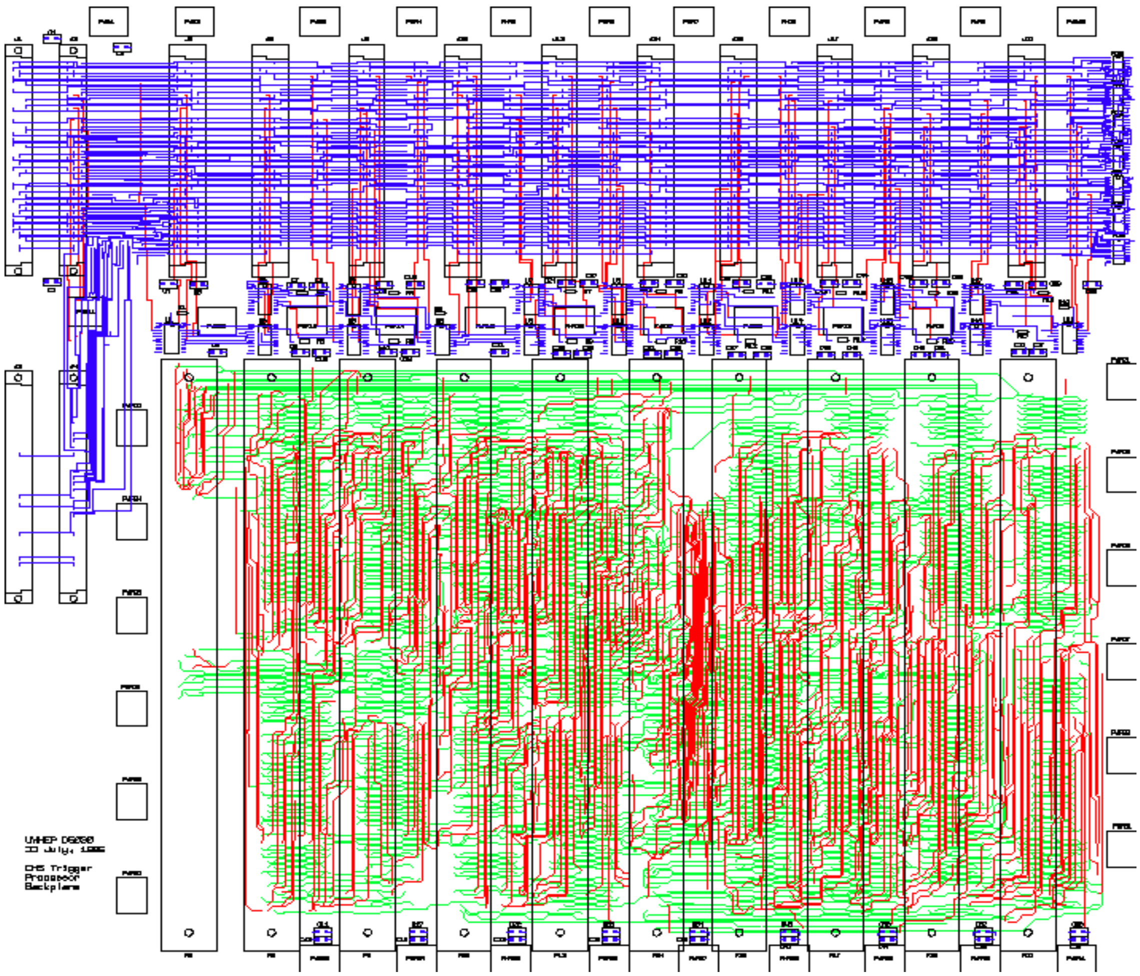
Backplane Prototype

Display of 3 out of 5 signal layers:

(most signals are hidden by top layer)

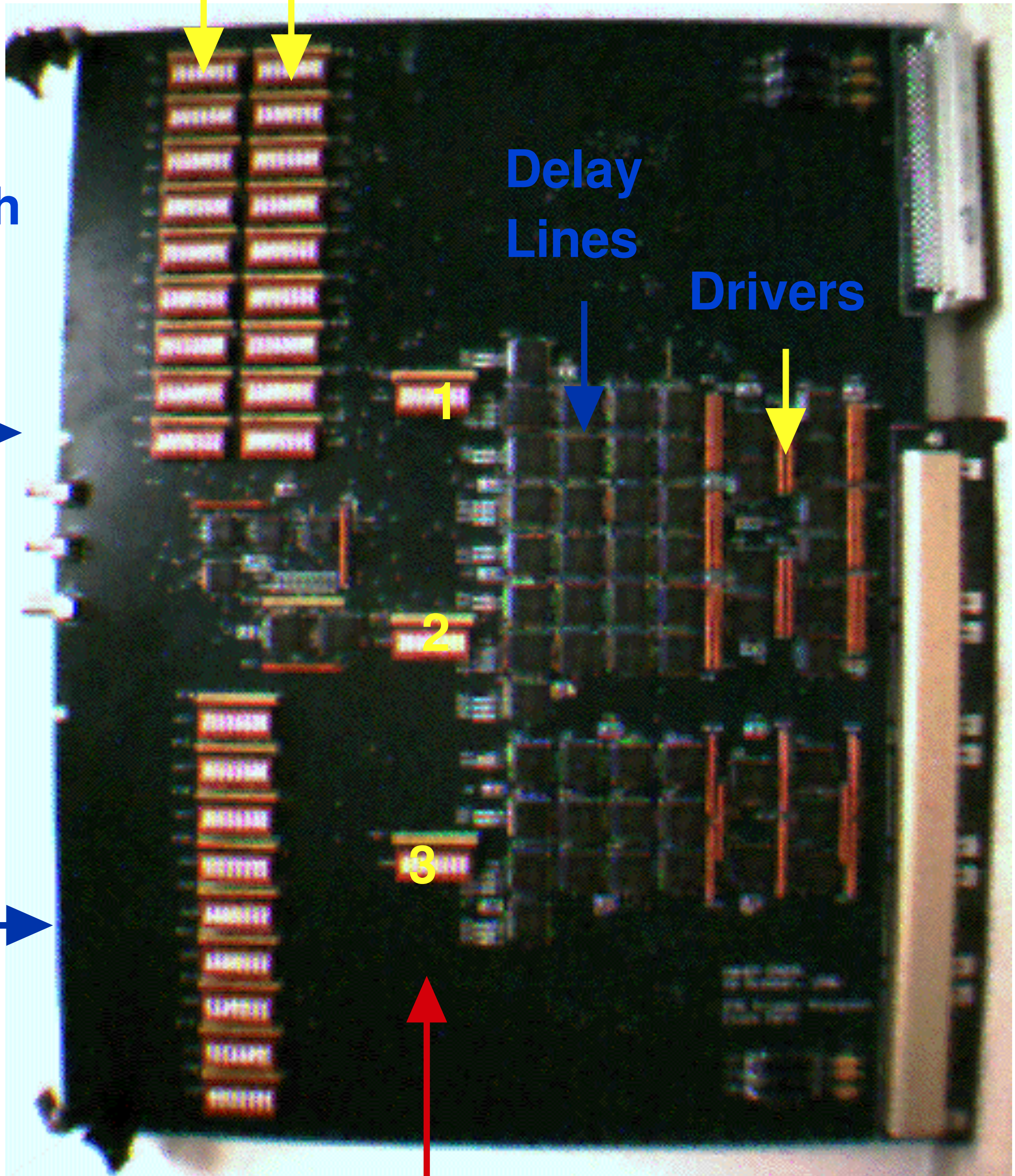


View of prototype backplane installed in prototype crate

Prototype Clock Board

switches to set delay lines

synch
&
reset

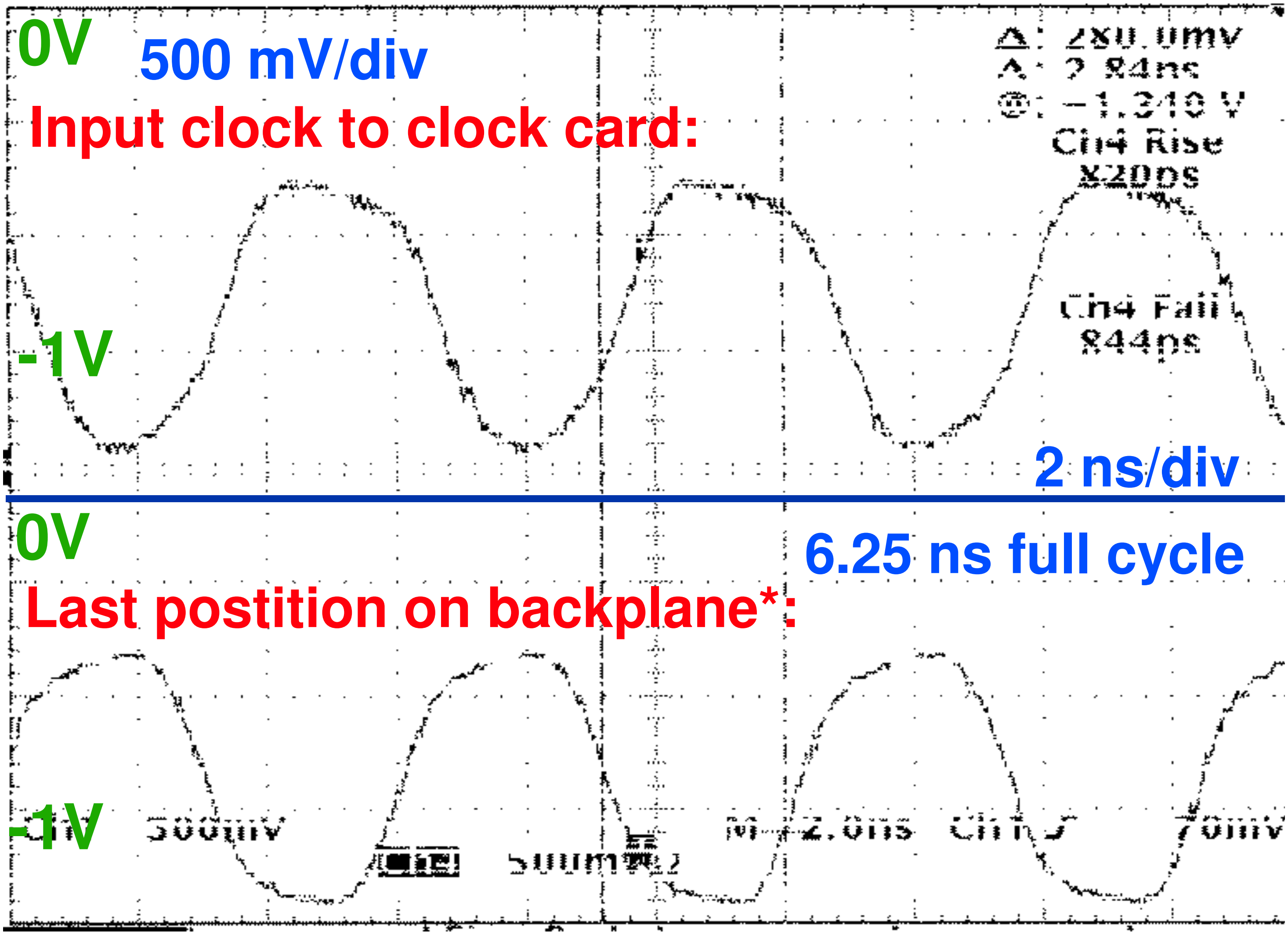


clock

1:Rcvr-E.I. 2:clk-synch 3:clk-reset

4 Recvr Cards, 4 Electron Iso, 1Jet/Sum

Backplane Test Results



*one side of differential pair

Conclusions:

- Output of backplane rise 820 ps
- Output of backplane fall 840 ps
- Measured 20% to 80%

Receiver & Pseudo -Electron Isolation Card Status/Plans

Receiver Card:

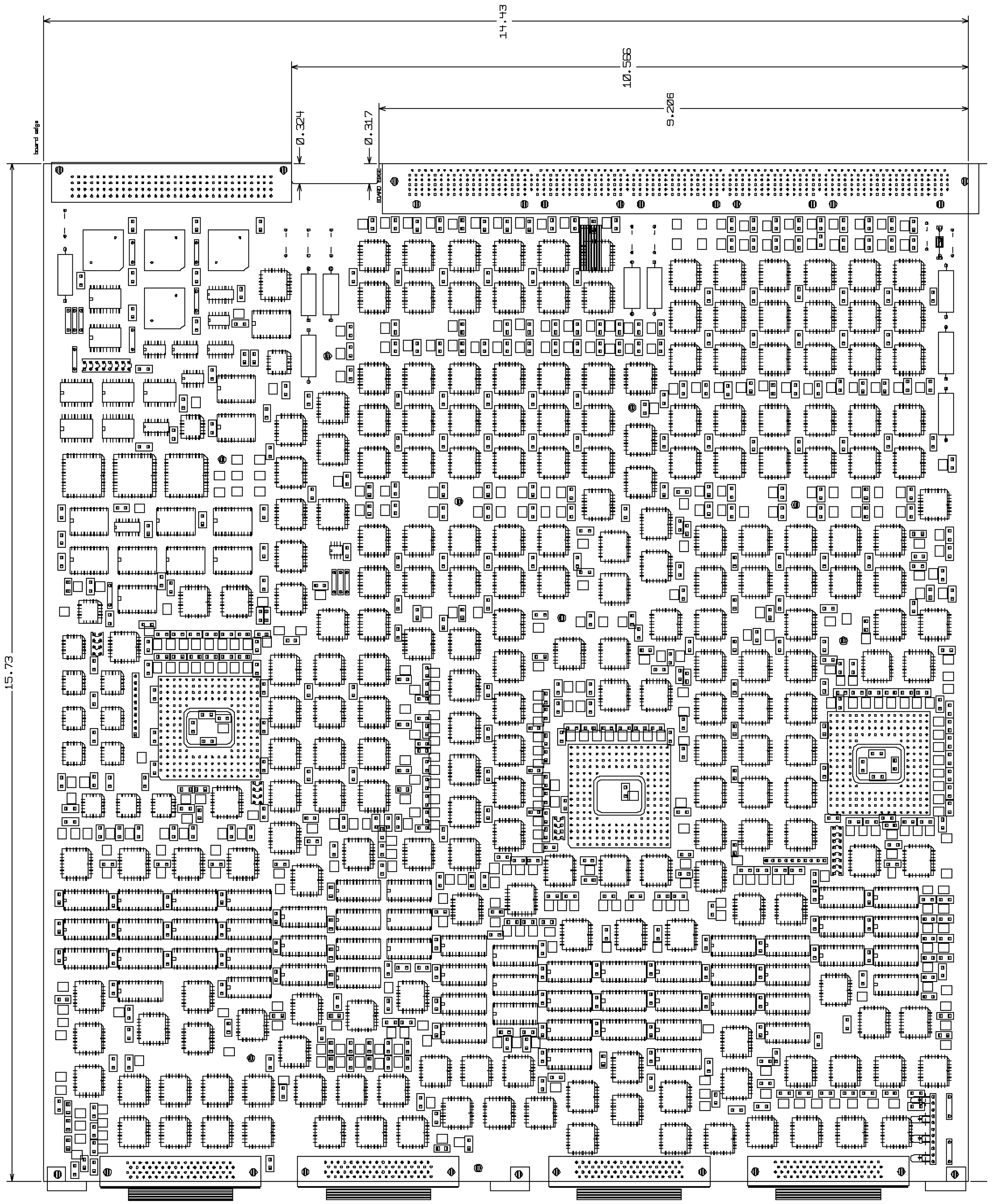
- Design & Layout finished
- Routing in progress
- Artwork generation & Quotes in May
- Manufacture in June
- Assemble in July
- Test & Evaluate July - Aug

Pseudo-Electron Isolation Card

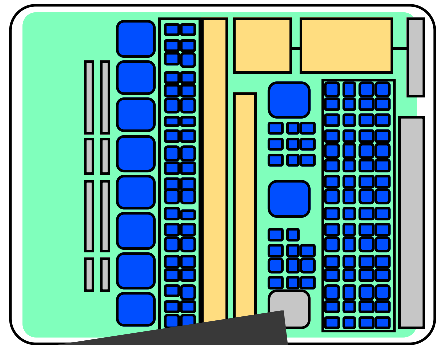
- Conceptual design finished
- Detailed design starts in May
- Finish Schematics in June
- Layout in July
- Board delivery in August

Full Backplane tests start September

Prototype Receiver Card Layout



Adder ASIC



ECL Input/Output - 8 channels

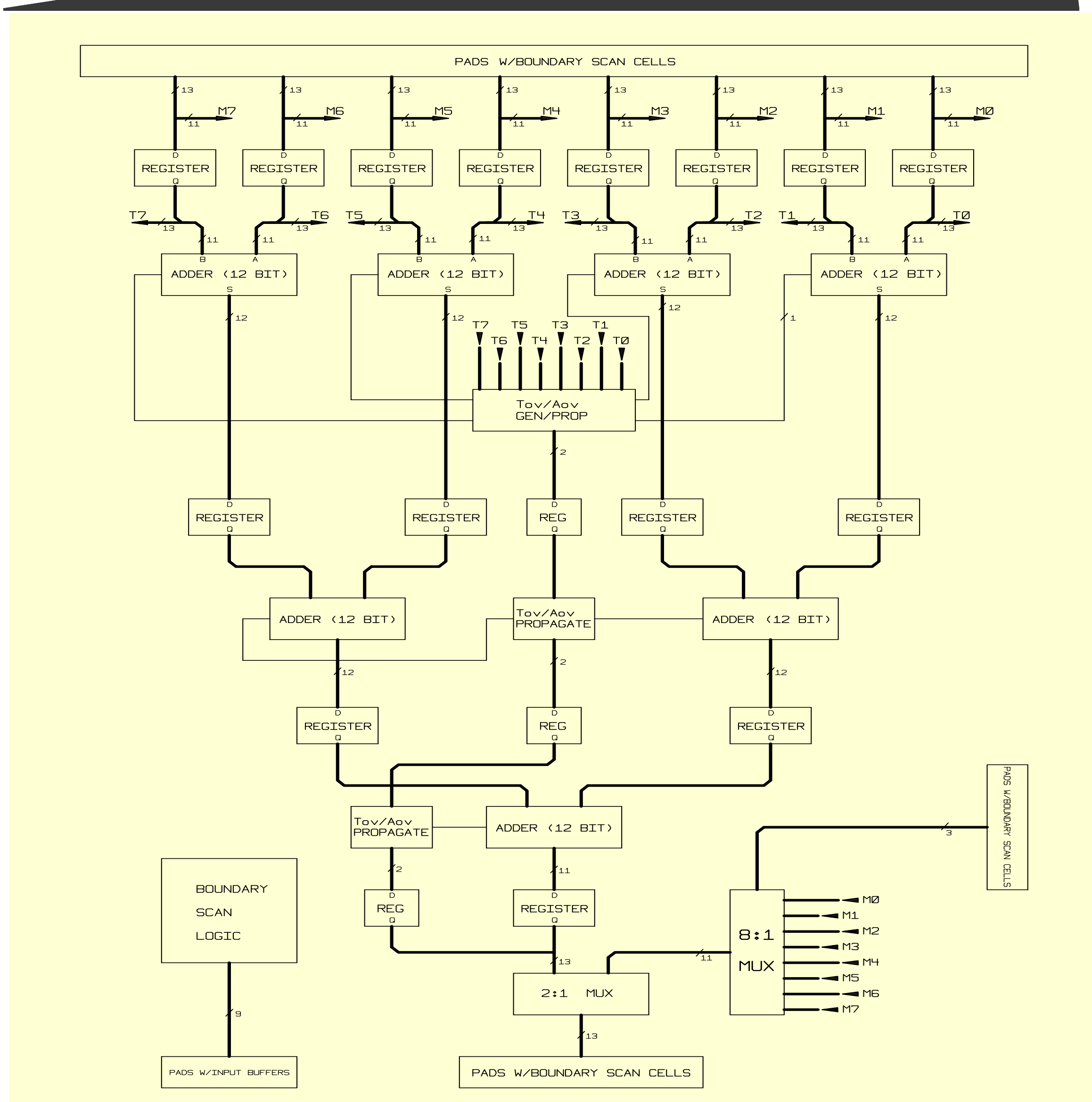
- 13 bit operand
- 10 Bit data + sign + Tower and arithmetic overflow

Latency of 25 ns when used at 160 MHz

Full boundary scan support

Built by Vitesse

- ~11000 cells; 4 Watts
- Tested at 200 MHz



Physics at high luminosity

Trigger Type	Trigger Et Cutoff (GeV)	Rate (kHz)		
		Individual	Cumulative	Incremental
Sum Et	400	0.48	0.48	0.48
Missing Et	80	1.29	1.7	1.22
Single Electron	25	6.84	8.34	6.64
Double Electron	12	1.45	9.52	1.18
Single jet	100	2.06	10.7	1.16
Double jet	60	2.17	11.6	0.93
Triple jet	30	3.16	13.3	1.7
Quadruple jet	20	2.96	14.3	1.01
Jet + Electron	50 & 12	1.35	14.9	0.59

Process	Efficiency (%)
H (80 GeV) ---> $\gamma\gamma$	97.4
H (120 GeV) ---> Z Z ---> e e μ μ	76.4*
H (200 GeV) ---> Z Z ---> e e j j	99.1
p p ---> t t ---> e X	88.3
p p ---> t t ---> H_+ X ---> t X	81.7
SUSY CMS TP Scenario A (M_{LSP} = 45, M_{spart} ~ 300 GeV)	83.0

*Inclusion of muon trigger provides full efficiency

Luminosity = 10^{34} cm^{-2} s^{-1}

QCD Background

The sum and missing E_t cutoffs are chosen to provide a 2 kHz rate. Electron/photon triggers are emphasized, with about 8 kHz rate out of total available 15 kHz. The remaining 5 kHz is available for jet triggers.

Signal Efficiency

High efficiency for all channels with electrons and photons.

The difficult-to-trigger top decay events have high efficiency, enabling studies of associated Higgs production.

Physics at low luminosity

Trigger Type	Trigger Et Cutoff (GeV)	Rate (kHz)		
		Individual	Cumulative	Incremental
Sum Et	150	1.04	1.04	1.04
Missing Et	40	2.11	2.82	1.78
Single Electron	12	10.3	12.3	9.5
Double Electron	7	1.54	13.1	0.764
Single jet	50	1.98	13.5	0.42
Double jet	30	1.63	13.9	0.422
Triple jet	20	1.02	14.1	0.178
Quadruple jet	15	0.68	14.2	0.077
Jet + Electron	15 & 9	5.98	15.2	1.02

Luminosity = 10^{33} cm^{-2} s^{-1}

QCD Background

The sum and missing E_t cutoffs are chosen to provide a 2 kHz rate. Electron/photon triggers are emphasized, with about 10 kHz rate out of total available 15 kHz. The remaining 3 kHz is available for jet triggers.

Process	Efficiency (%)
p p ---> t t ---> e X	99.3
p p ---> t t ---> H+ X ---> t X	99.0
p p ---> b b (hadronize), B ---> e X	0.2 (But 400 Hz)
SUSY CMS TP Scenario A (M_{LSP} = 45, M_{spart} ~ 300 GeV)	97.8
SUSY Neutral Higgs (Range of tan b and M_H values)	45 - 98

Signal efficiency

High efficiency is realized for the benchmark processes involving top decays and SUSY sparticles.
A dedicated tau trigger is under study to improve efficiency for low mass range of SUSY Higgs.
There is also high rate of B signal in level-1 sample.

Conclusions

A sophisticated hardware trigger system is required to study physics with CMS at LHC.

A series of simple algorithms to trigger on electrons, photons, jets and missing energy are identified.

Multiple levels of programmable cuts for the electron/photon trigger allows for optimization of the trigger system at the time of data taking.

Conceptual design of calorimeter trigger system including trigger primitives generation on front-end, and regional trigger system with custom backplane for data sharing and integrated circuits for processing is complete.

Front-end trigger primitive generation including fine-grain EM ID was demonstrated to work in test beam.

The prototype custom backplane with 160 MHz point-to-point links shows good electrical characteristics - Better than 1 ns rise and fall times seen on longest paths.

Adder ASIC, built in Vitesse's GaAs process, is tested to perform at 200 MHz well above the 160 MHz requirement.

Backplane and card test setup is in progress.

High P_t physics studies using CMS at LHC are feasible due to the design of trigger and DAQ system presented.