The Application of the AutoBahn Chip for Building a High Bandwidth, Low Latency Network of PCs or Workstations

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AutoBahn is a new high speed, serial interconnect technology originally designed as a serial bus for VME backplanes. It may be used also to implement uni- or bidirectional serial links. Based on that technology a PCI to AutoBahn interface module was designed which enables the implementation of ring based networks of PCs or workstations. In this design the high data transfer bandwidth of AutoBahn is combined with special hardware to achieve low latency communication.

Key words: PCI, AutoBahn, Fast serial links, Low latency communication, PC and workstation networks

1 Introduction

Today's computer applications demand a nearly unlimited bandwidth and low latency communication. Existing solutions are either low latency, low bandwidth (ETHERNET, FDDI) or quite expensive (ATM, FCS).

To serve the demand for high bandwidth data communication in computer and telecommunication environments Motorola introduced in 1994 a new serial bus concept - AutoBahn. Originally designed as a high bandwidth serial bus for VME backplanes to maintain high speed data exchanges (e.g. for video applications), AutoBahn technology can also be used to implement point-to-point serial links.

2 AutoBahn Overview

The Autobahn device MC100SX1451 [1] provides to the user an interface between a 16 or 32 bit wide parallel bus system and a differential serial line which uses positive ECL (PECL) technology to transfer data.

The main architectural features of AutoBahn are:

- High bandwidth serial bus or serial point-to-point link
- Burst transfer rates of: 450, 900 (now) and 1800 (near future) MBit/s which corresponds to 50, 100, 200 MByte/s
- Variable data transfer rates: fixed burst transfer rates are combined with gaps in the data flow if no new data is written into the transmit register prior to the completion of a serial data burst
- 16/32 bit interface to a parallel bus system or other data sources
- Absence of a sophisticated transfer protocol, e.g. packets. The data transfer is nearly overhead free with only one synchronization bit for every byte.
- On-chip clock recovery and data synchronization
- Single chip solution for both sending and receiving data

The AutoBahn device supports three modes of operation: Idle, Transmit, Receive.

- After reset the device is in Idle Mode. The serial bus is cut off and the receiver part of the device is listening to detect a bus activity.
- The Transmit Mode is entered after data has been written into the parallel data register. The device transfers the data from the parallel data register to the serial transmit register, inserts framing information and shifts the data out.
- In Receive Mode the device strips off the framing information and clocks the data into the serial receive register. After a full word has been received the data is transferred to the parallel receive register and a FULL flag is activated.

3 The AutoBahn Evaluation Board

To test the special features of the new serial data transfer technology as well as to measure some additional parameters, a VME based AutoBahn evaluation system for point to point communications was developed at DESY Zeuthen. This module consists of four identical channels. Each of them is connected via a fast synchronous SRAM (Pentium Cache RAM) to the onboard VME interface and can be programmed to act as a transmitter, a receiver or a receiver with built-in data comparing facility [2]. The fast SRAM serves as a data buffer to match the different bandwidth of the VME interface and AutoBahn.

With this board, some measurements have been performed using 50 cm and 3 m coax cables to interconnect two channels. In the case of the 3 m cable the delay from writing to the AutoBahn transmitter to the moment when the data is ready at the receiver side is ca. 100ns (internal chip delays + 32 bit word transfer time + cable delay) for the first word transferred and ca. 85ns for all following data words (device runs below the max. transmission speed) respectively 40ns (device runs at the max. transmission speed). Next tests will include data transfer using different cables as well as long term stability (measuring bit error rates).

4 PCI to AutoBahn Interface Module

The transfer rate of AutoBahn (100 MByte/s now, 200 MByte/s soon) corresponds very well to the bandwidth provided by the PCI bus (max. 132/264 MByte/s for 32/64 bit data bus). On the other hand the PCI bus is now a building block in a modern workstation or PC.

As a result of a collaboration between DESY Zeuthen and INFN Pisa and Rome a PCI to AutoBahn Interface Module (Fig. 2) was designed which provides the basis to build a high bandwidth, low latency network of PCs or workstations interconnected in a 2D ring architecture (Fig. 1). In this design, the high data transfer bandwidth of AutoBahn is combined with special hardware to achieve low latency communication.

Data Transfer Principles:

In the ring structure, one Master is connected to one or more Slaves. Each interface module (Master and Slave) has two buffers, one for receiving data (RxFIFO) and one for transmitting data (TxFIFO). This FIFO structure makes it possible to pipe data together with Control/Status information.

Data is transferred in the form of packets. Each packet is framed by a Header and an End Of Packet (EOP) terminator. To distinguish between data and control information in the data stream a word stuffing mechanism is implemented in hardware. If in the data stream the code 0xffffffff is present then:

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if NEXT_DATA == 0x00xxxxxx
   then PREVIOUS_DATA is DATA (0xffffffff)
   else NEXT_DATA is CONTROL/STATUS information
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Based on that protocol the following commands and status messages are implemented in hardware:

Abbr.	Code	Description	Used by
DNC	0	Data, No Control, the 0xffffffff word is a data word	master/slave
GWR	1	Header, Global Write (Broadcast)	master
		followed by 32 Bit Packet No. + Packet Length	
LWR	2	Header, Local Write	master
		followed by 32 Bit Packet No. + Packet Length	
GRD	3	Header, Global Read	master
LRD	4	Header, Local Read	master
RFS	5	Header, Read From Slave	slave
		followed by 32 Bit Packet No. + Packet Length	
EOP	6	End Of Packet,	master/slave
		followed by a Checksum (32 bit XOR)	
EOG	7	End Of Global transfer	master
TOK	8	Transfer O. k.	master/slave
TFS	9	Transfer Failed, no Space (FIFO full)	master/slave
TFC	10	Transfer Failed, Checksum error	master/slave
RTO	11	Read Timeout	slave
WHO	12	Registration of all Slaves in the ring	master
GRES	13	Global Reset	master
LRES	14	Local Reset	master
GNT	15	Grant, Master token	master

A detailed description of all commands including formats and state diagrams is contained in [3]

The PCI to AutoBahn interface card will run under standard operating systems, e.g. LINUX. Preliminary work for driver development has been carried out. A LINUX driver for a similar board with the same PCI interface is ready and in use now [4].

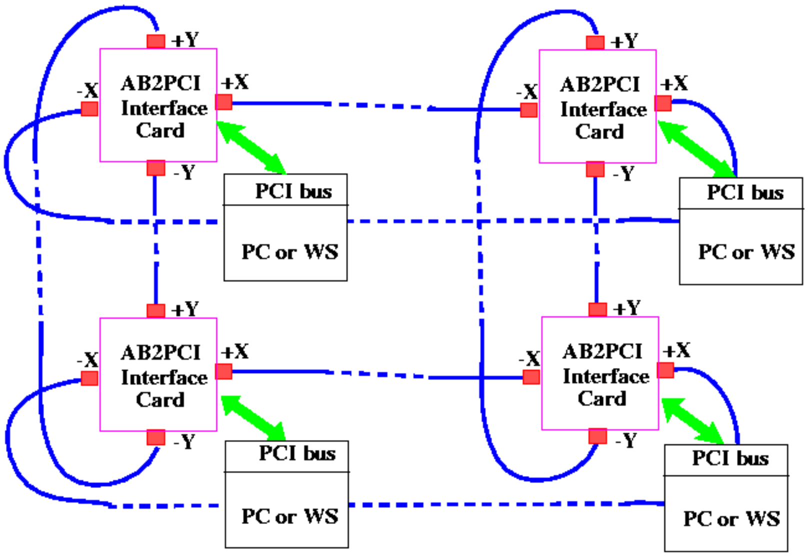

Fig. 1. 2D PC or Workstation Network based on AB2PCI Interface Card

5 Conclusion

AutoBahn is a new technology for high bandwidth serial data transmission. The absence of a sophisticated transfer protocol provides to the user the possibility to implement protocols optimized for specific applications.

An AutoBahn evaluation board was built to test specific interface features and to perform speed and latency measurements. Based on that experience a PCI to AutoBahn interface card with four channels has been designed which allows to build a high bandwidth, low latency network of PCs or workstations. A simple protocol implemented in hardware is the key for low latency communication.

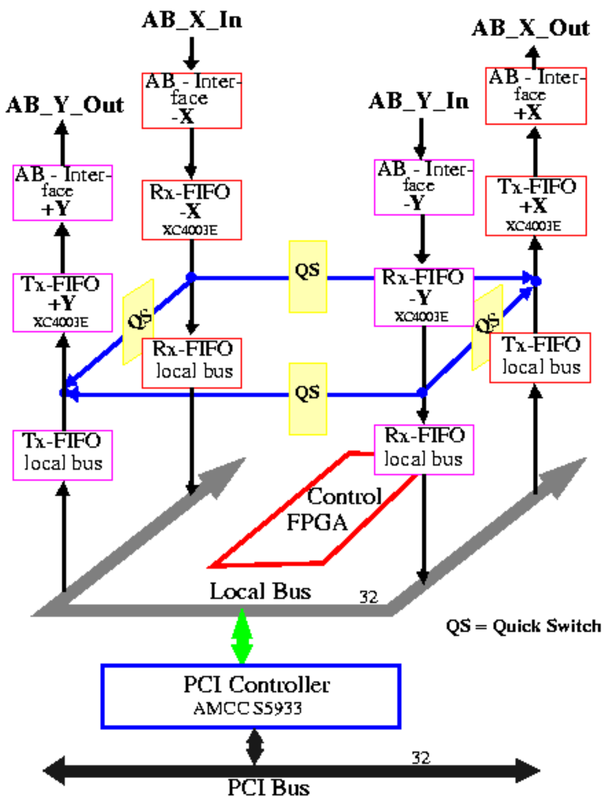

Fig. 2. AutoBahn to PCI interface Module

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