High Performance Computing Nodes using a DEC Alpha Processor and a T9000 Transputer

R.W. Dobinson [a,b], S. Fisher [b], R. Heeley [a], P.D. Maley [b]

[a] *CERN, Geneva, Switzerland*

[b] *Liverpool University, England*

1 Introduction

A high performance computing node has been designed using a T9000 Transputer as a communications controller for a DEC Alpha microprocessor. Such a hybrid node combines the computational performance of the Alpha with scalable the communications capabilities of the T9000 into a so called TransAlpha Module.

This paper presents a brief description of the TransAlpha module and a discussion of its computational and communications performance. Two applications of the module in HEP are presented: on-line event reconstruction in CPLEAR and R&D work for the ATLAS level-2 trigger which is currently in progress.

2 The TransAlpha Module

A block diagram of the TransAlpha module is shown in figure 1. The major components are:

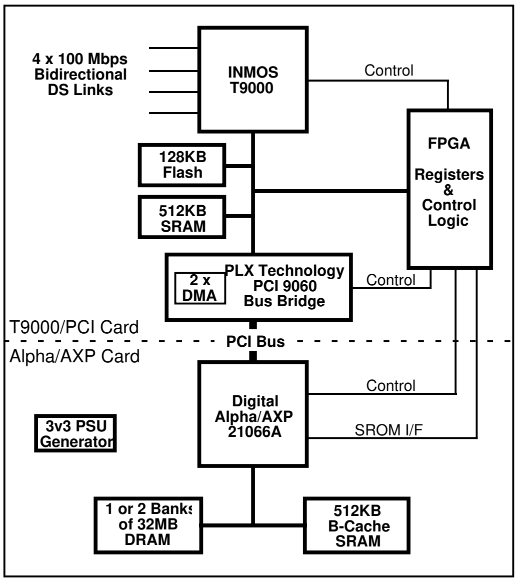

Fig. 1. Physical layout of the TransAlpha Module.

- A 233MHz 21066A DEC Alpha with 512 KBytes of second level cache and 32 or 64 MBytes of DRAM. This chip has an on-chip PCI IO controller connected directly to a PCI bus.
- A 20 MHz T9000 Transputer with 512 KBytes of SRAM on its local bus. The T9000 has four on-chip engines for driving IEEE 1355 DS links.
- A PLX PCI 9060 chip acting as a bridge between the PCI bus and the local bus of the T9000.

Preprint submitted to Elsevier Preprint *3 March 1997*

– An FPGA providing glue logic between the local bus of the T9000 and the PCI 9060 chip.

Both processors have full access to all memory via either their own local bus or the PCI bridge. Access is either via single word read and writes or via DMA transfers. DMA transfers are performed by the 9060 chip which has two independent DMA engines. These are controllable from either processor. Interrupts may be sent to either processor from the other via doorbell registers in the 9060 and interrupts may also be sent on completion of DMA transfers. The module conforms to the INMOS HTRAM specification and can thus be plugged directly into an existing Transputer-based system.

The Alpha processor runs no OS or micro kernel and so is restricted to single threaded code. It is programmed in C and a library of synchronous and asynchronous communication functions are provided to facilitate parallel computing. Message passing between the Alpha and the rest of the network are performed by a server process on the Transputer. The DMA engines in the 9060 transfer data between the Alpha's memory and the T9000's local memory. Hardware in the T9000 sends and receives data on the DS links.

3 Performance

The main flaw with the T9000 processor is its lack of processing power. Several standard benchmarks have been run on the TransAlpha module (e.g. Rinf1, Poly1 and Poly2 from the PARKBENCH codes).

Benchmark	25MHz T9000	TransAlpha (233MHz Alpha)
Rinf1	1.5	14.5
Poly1	5.1	37.0
Poly1	5.1	26.6

These show a factor seven improvement over the Transputer processor alone. The TransAlpha module performs at about 60% of a similar speed Alpha workstation due to its slower effective memory speed.

Transputer communications are built around the concept of virtual channels: process to process data paths. Many virtual channels can be placed on a single DS link, but the link becomes saturated by any more than three active virtual channels.

The communications performance of two TransAlphas is compared to that of two T9000s. Throughput is shown for 2 KByte messages transfered to and from external, i.e. not on-chip, memory.

Uni-directional send	T9000→T9000	TransAlpha→TransAlpha
Single Virtual channel	4.6 Mbytes/s	4.5 MBytes/s
Three Virtual Channels (single DS link)	6.3 MBytes/s	5.2 MBytes/s
Twelve virtual channels (four DS links)	16.5 Mbytes/s	12.2 Mbytes/s

4 Applications

A farm of 54 T9000 Transputers was integrated into the CPLEAR experiment at CERN with the aim of doing the off-line reconstruction in real-time. The Transputers were unable to provide the necessary computational performance partly owing to the low achieved clock speed. A test-system with two TransAlpha modules replacing some of the T9000 nodes in the system was built and run.

This test system ran without problem for several days processing over two million events. Extrapolating the results to a full size system, the real-time reconstruction could have been performed with a farm of twenty-five TransAlpha modules, compared to the 250 T9000s that would have been needed.

Our present work with the TransAlpha modules is the building of a demonstrator for the ATLAS Level-2 trigger and is shown in figure 2.

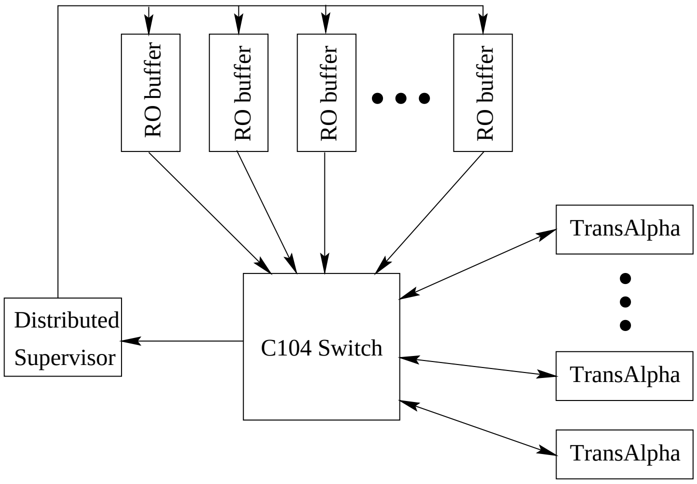

Fig. 2. ATLAS Local-Global trigger demonstrator.

Each TransAlpha performs one of two functions:

- The collection of event fragments from detector read-out buffers followed by the execution of feature extraction algorithms – local processors.
- The collection of features from the local processors followed by their analysis and a trigger decision – global processors.

This application requires both computational power and performant inter-processor communications. Both are provided by the TransAlpha module.

5 Conclusions

A high performance computing node based on a DEC Alpha with a T9000 transputer acting as a communications processor has been developed. Several of these nodes have been and are presently being used successfully in real-time HEP environments. Further information can be found in: CERN/ECP 96-18 “High Performance Computing Nodes for Real Time Parallel Applications”

6 Acknowledgements

We gratefully acknowledge the support provided by the Particle Physics and Astronomy Research Council, PPARC, and Professor E. Gabathuler, Liverpool University, for their interest in and support of this project.