# CTTS: The Composite Timing and Trigger System of the JET machine

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The Composite Timing and Trigger System (CTTS) has been developed for distributing real-time marks, triggers and auxiliary commands throughout the JET plant, allowing synchronised operation of a mixed set of front-end processors (VME, CAMAC, PC). This paper outlines the general architecture and gives a short description of the principal components.

*Key words:* Trigger systems; Control and Data Acquisition

## 1 Introduction

The Joint European Torus (JET) is the major project in the European nuclear fusion programme. JET operates the largest tokamak device in the world for studying the magnetic confinement of plasmas in condition close to those required by a fusion reactor. The Control and Data Acquisition Systems (CODAS) Division [1], is responsible for the fully integrated computer-based system which is essential for the operation of the tokamak itself, auxiliary equipment and diagnostic devices. CODAS equipment is scattered over an experimental area of 300x300 metres, with a total of more than 70000 I/O points. Data collection for a single machine pulse exceeds 300Mb.

CODAS is built around clusters of UNIX computers (SUN Sparc-stations), one for each of the major JET subsystems. These host computers are connected, through a network of switched Ethernet segments and CAMAC Serial Highway loops (IEEE-595), to over two hundred front-end processors. During a JET pulse, lasting for around 60 seconds, there is need to synchronise actions and trigger data acquisition with a much higher precision than the aforementioned interconnections would allow. Hence the necessity for an additional medium able to provide the required accuracy.

At the beginning of JET activity, in 1983, when only CAMAC front-ends were deployed, the problem was tackled by using a hierarchy of programmable timer units, the Central Timing System (CTS) [2], feeding an independent distribution network for each of the requested timing marks. A similar approach was also used for the transmission of asynchronous real-time triggers (RTTN). The introduction of VME front-ends, in 1993, made clear that the old arrangement could not easily match the requirements of the new applications being developed. It was therefore decided to devise a new timing system that, although maintaining full compatibility with the large number of CAMAC installations, could better satisfy the timing needs of the VME environment. Additional decisions influenced also the early design phase. The first was to avoid the use of specialised encoder/decoder chips, allowing the basic decoding function to be implemented as a relatively low gate-count macro in a FPGA. The second was to be compatible with 62.5/125 $\mu$ fibres and RS-485 electrical links, as well as with a pre-existing distribution network based on 200 $\mu$ PCS fibres. Due to this original commitments, the Composite Timing and Trigger System (CTTS) differentiates itself from several other multiplexed timing systems for control of tokamak devices [3–5] that have all a common origin in the CAMAC-based approach developed for the Princeton TFTR experiment [6].

## 2 The CTTS Signal

CTTS is based on the continuos transmission, from a single centralised encoder, of a composite signal which is embedded, by pulse width modulation, in a 2MHz reference clock. A dual level multiplexing scheme is employed, providing basic resolutions of 40 microseconds, for asynchronous real-time triggers, and 1 millisecond, for pre-set CTS milestones and other messages. In addition to the main broadcast mode, it is also possible to transmit special commands to individually addressed VME targets.

The signal structure is presented in Fig.1: 25 frames, of 10 bytes each, are grouped to form a data unit. The 8-byte payload of each frame is divided into two 32-bit fields. The first field, with the exception of bit-0 and bit-1 used as special markers, always carries a pattern corresponding to the status of the 30 supported real-time triggers (1 is perceived as an active trigger). The meaning of the second field varies with the position of the frame in the data unit: pre-set milestones are included in frames 23 and 24, a time stamp message is in frame 0, while frame 1 is reserved for addressable commands. The remaining frames are available for future extensions. Primary distribution takes place over a star-shaped fibre-optic network. Secondary optical branches are supported via repeaters, with RS-485 multi-drop configurations of limited length also allowed (Fig.2)

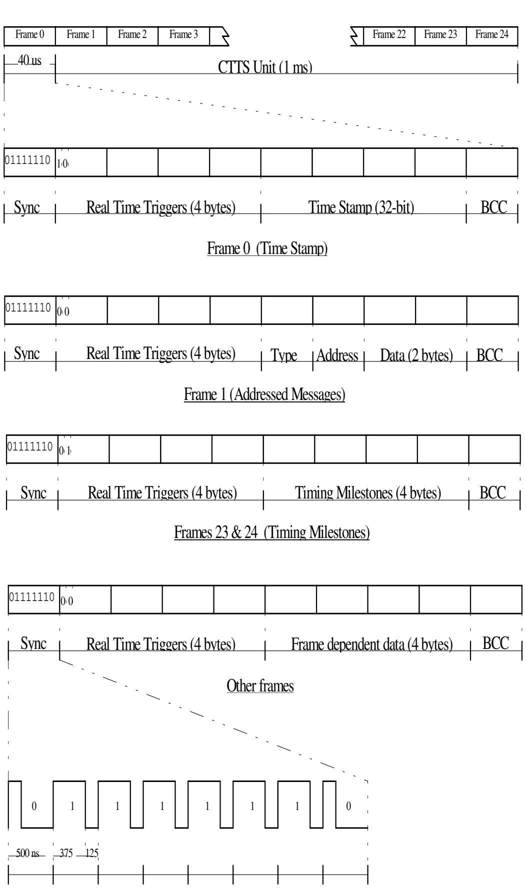


Fig 1 - CTTS Signal Structure

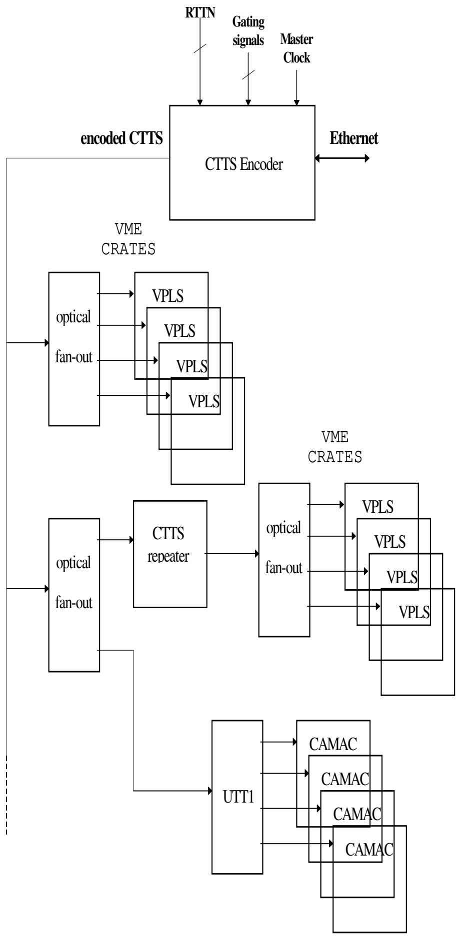


Fig 2 - CTTS Signal Distribution

## 3 System Components

The introduction of CTTS has required deployment of highly integrated hardware and software components, developed according to JET CODAS Division standards. These include the Xilinx X4000 FPGA family for logic boards design and the VxWorks real-time operating system. Xilinx code has been produced within the Xact development environment using both Abel hardware description language and schematic capture techniques.

### *3.1 CTTS Encoder*

The Advanced CTTS Encoder (ACE) is a 6U single-width VME module, combining a commercial processor (Eltec SAC-30, 68EC030 CPU), and a Xilinx based logic board. The application firmware and the Xilinx code are locally held in ROM. The FPGA control and data registers are mapped into the local processor addressing space, while communication over the VME bus is via the SAC-30 dual-ported RAM. Main functions include: generation and gating of pre-set timing milestones, sampling of external asynchronous triggers, processing of addressable messages, time-stamp insertion, data formatting and modulation.

### *3.2 VME Decoder*

CTTS decoding for VME-based applications is carried out by the VME Service Module (VPLS), a standard element in CODAS VME racks, which also supports a variety of other unrelated tasks. The physical structure is similar to that of the encoder, but with a different logic board. The CTTS content is decoded and copied to a shared memory area: both current and accumulated information (event recording) is made available. Selected timing marks and triggers are routed to the rear P2 connector and can also be used for generating VME bus interrupts.

### *3.3 General Purpose Decoder*

The Universal Timer and Trigger (UTT1) is a stand-alone FPGA-based module in 3U Eurocard format. It is mainly used as CTTS decoder for non-VME systems such as CAMAC and PC. It can also be re-programmed for other functions by adapting the Xilinx code. A special configuration is used as CTTS signal repeater.

## 4 Mode of Operation

At JET, the control software is hierarchically organised in a three- level structure. The lowest level, the device driver, provides abstraction from the hardware by translating inputs and outputs into logic point-names uniquely defined in the "hardware-tree" database. The second, or subsystem level, is responsible for the integrated control of groups of logically related components. Finally, the JET Supervisory level (level-1) co-ordinates all subsystems using a method based on state transition diagrams.

The CTTS control software is integrated in this structure. During the preparation phase for a JET pulse, the subsystem responsible for the timing reads the Milestone pattern required for the next pulse and transfers it to the central CTTS encoder via a TCP/IP based message protocol. The positive completion of this operation is notified to the Supervisory level. When a start-of-pulse is requested, and all the subsystems are reported as ready, a corresponding command is sent to the ACE module, which then runs the sequence autonomously under control of the local CPU. The overall timing distribution process is constantly monitored: the information collected, including full event logging and statistics for all the components involved, is displayed on mimics.

## 5 Conclusions

CTTS started to operate in January 1994. It is now well established at JET and provides a common triggering source for all JET front-end processors, including more than 40 VME-based. We believe that the initial design goal has been substantially achieved, combined with a good reliability record, as required for any element essential to the operation of the machine.

## References


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