Report on the ALICE Detector Data Link: method used, protocol and design status

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ALICE COLLABORATION

The future LHC experiments are planning to use more than 200.000 links for the connection of the different layers of the front-end electronics (FEE) and the data-acquisition system. There are several applications where industrial products can be used. However, in case of specific requirements special solutions are needed by the experiments. CERN, RMKI and BME are developing a new link (called detector data link or DDL) for the special needs of the ALICE experiment. This link will provide high-speed transmission of data blocks (e.g. event data, thresholds, pedestals) in both directions between the FEE and the data-acquisition system. The DDL can also be used as a transmission medium for the remote control of the FEE during the normal operation and for the remote debugging during the system integration of the ALICE detector. In this paper we present the concept of the DDL and the methods used for its development.

1 Introduction

The ALICE [1] detector data link (DDL) will interface the front-end electronics (FEE) of all the sub-detectors to the read-out receiver cards (RORC) of the data-acquisition system. The source interface units (SIU) are connected to the FEEs and placed inside the detector. The destination interface units (DIU) are connected to the RORCs, located in the counting room about 200 meters from the detector. The two DDL interface units are connected through the physical medium which is a duplex optical fibre. The complete ALICE data-acquisition system will consists of about 700 DDLs. Figure 1 shows the DDL concept.

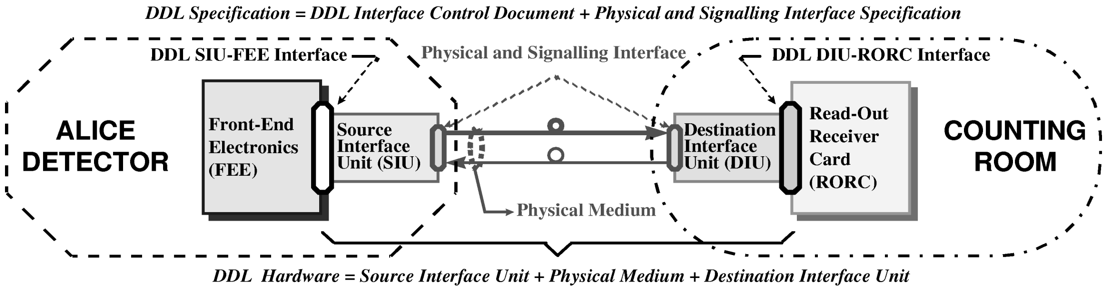

Fig. 1. The DDL concept

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2 Development Method

A formal approach is being followed for the specification and development of the DDL. The ESA PSS-05 software engineering standard [2] has been used for the preparation of the User Requirement Document [3], the Interface Control Document [4] and the Physical and Signalling Interface Specification Document [5].
The LOTOS formalism [6] has been chosen for the formal description, simulation and verification of the DDL protocol The VHDL hardware description language [7] is being used for the simulation of the DDL.

2.1 User Requirements

The main data flow will take place from the FEE to the RORC. The 700 DDLs shall transmit in total 2.5 GByte/s event data from the FEE to the RORC with a detected bit error rate of $< 10^{15}$. Each DDL shall be able to transmit data at a rate of 100 MByte/s. As the zero suppression algorithm requires downloading blocks of data into the FEE, a throughput of 10 MByte/s is needed in the opposite direction.
Both the FEE and the SIU shall be remotely controlled by the RORC through the DDL, since their placement inside the detector will not allow using any other cabling apart from the DDL medium. Therefore commands and status information shall also be transmitted between the FEE and the RORC. Figure 2 shows the required information transfer between the DDL and the external systems.

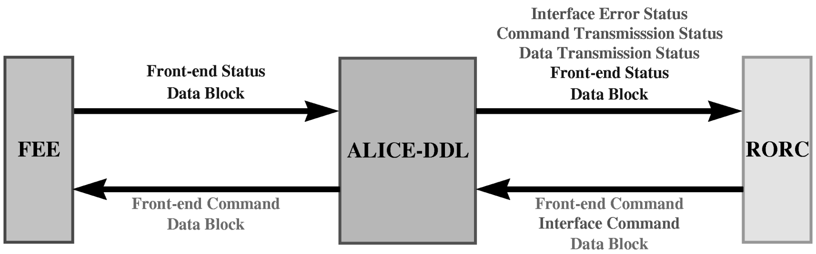

Fig. 2. The information transfer between the DDL and the external systems

Since the SIU is located inside the detector, the requirements for the lifetime (> 10 years), the power consumption (< 5W) and the footprint (< 50 cm^2) of this unit are key issues. More strict requirements have been identified for the ITS sub-detector [1] where radiation tolerant electronics is needed and the maximum footprint of the SIU shall be less than 15 cm^2.
To achieve the high reliability of the experimental apparatus, efficient test of all the sub-systems shall be provided. The DDL shall allow to test the FEE remotely by using JTAG Boundary-scan Testing procedure [8]. The DDL itself shall also have a powerful self-test mode.

2.2 Interface Specification

The FEE-SIU and RORC-DIU interfaces are described in the Interface Control Document. The definition includes the physical and electrical description of the interface units, the interface signal description, the definition of the information structures, the interface protocol and the interface timing.

2.3 Physical Medium Specification

In the physical and signalling interface specification the different layers of the communication protocol on the physical medium have been described. The Fibre Channel standard (FCS) has been chosen [9] For the first implementation. The choice of FCS was motivated by its very robust physical and coding layers and by the availability of cheap high-performance components.

2.4 Protocol Simulation and Verification

One of the most important phases of the DDL development is the test of the data transmission protocol used between the FEE and the RORC. It allows us to verify whether:

- the protocol is capable of serving all the requirements of the information transfer;
- the protocol is properly defined;
- there is any inconsistency or redundancy in the protocol.

We intend to study the DDL protocol using LOTOS: no deadlocks or endless cycles should occur on any error condition and the system should be able to recover from any illegal state after a given time-out period.
VHDL will be used to check whether the DDL level protocol can be mapped to the physical medium protocol and to study how the timing of the physical medium level information transfer influences the DDL level. The VHDL model will then be used in the digital system design and simulation phase of the DDL development project.

2.4.1 Formal Description of the DDL Protocol using LOTOS

The LOTOS language and the LOTOS tools are used for the formalisation and the validation of the protocol. The DDL protocol has been described in an informal way [6]. A validation model shall be constructed from this informal description. In the formal description of the DDL protocol, the FEE and the RORC are the service users and the DDL is the service provider. The ports between the SIU - FEE and the DIU - RORC will be defined as service access points. In the first design step (called physical decomposition) the FEE, RORC and DDL components will be specified as black boxes. These components will be defined as LOTOS processes with their mutual gates synchronised in all events (see Figure 3).

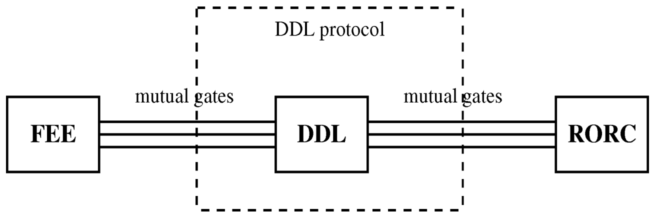

Fig. 3. The physical decomposition

The next design step is a functional decomposition of the black-box models and their interfaces into more complex (white box) models following the stepwise refinement process. The highest level procedures will be the data transmission protocol between the FEE and the RORC as well as the self-test protocol of the DDL. The highest procedures will use lower level processes which are the data block transmission protocol with flow control, the command transmission protocol and the status read-out protocol. For the validation of the formal description of the protocols, all the components must be able to generate no valid commands and data blocks as well as wrong or missing answers.

2.4.2 Simulation of the DDL by using VHDL

The VHDL hardware description language supports different abstraction levels to model digital electronic systems. In the DDL simulation, we three levels: the test environment, the signals of the DDL interfaces and the physical medium. The simulation model of the DDL is shown in Figure 4.

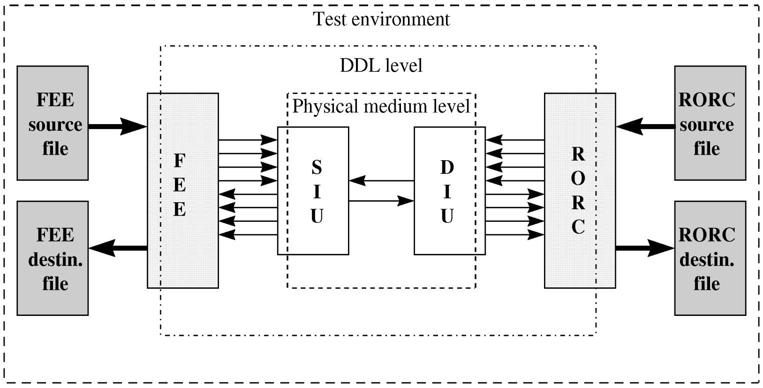

Fig. 4. Simulation model of the DDL protocol test

The physical medium level simulation is conforming to the DDL Physical and Signalling Interface Specification Document [5]. The test of the DDL includes the test of the physical medium. The physical medium layer shall carry all the information provided by the DDL layer. The DDL level simulation is conforming to the Interface Control Document [4]. The test environment provides a convenient way to control the information transfer on the DDL and to test the proper operation of the DDL signals. The stimuli are read from source files and the results are written to destination files on both sides of the DDL. The stimuli consist of combinations of commands and data blocks. The results consist of status words and data blocks according to the response of the simulation model.

3 Conclusions

The development phase of the DDL project has just started. Therefore it is too early to give conclusions on the usage of LOTOS and VHDL for the protocol design, simulation and verification. Our first experience with a formalised way of collecting user's requirements has been very stimulating. The definition of the interface has been an iterative process accomplished in close contact with the users.

4 References

References

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[5] ALICE-DDL Physical and Signalling Interface Specification Document; ALICE/97-04, Internal Note/DAQ, 14.02.1997

[6] LOTOS - Formal Description Technique based on the Temporal Ordering of Observational Behaviour, ISO/IEC 8807

[7] VHDL Harware Description Language; IEEE-1076

[8] Test Access Port (TAP) and Boundary-scan Architecture; IEEE 1149.1

[9] Fibre Channel Physical and Signalling Interface; ANSI X3.230-1994